

# DATA SHEET

## **TDA9852**

**I<sup>2</sup>C-bus controlled BTSC  
stereo/SAP decoder and audio  
processor**

Preliminary specification  
Supersedes data of 1996 Feb 28  
File under Integrated Circuits, IC02

1997 Mar 11

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

## TDA9852

### FEATURES

- Quasi alignment-free application due to automatic adjustment of channel separation via I<sup>2</sup>C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I<sup>2</sup>C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Power supply
- I<sup>2</sup>C-bus transceiver.



### GENERAL DESCRIPTION

The TDA9852 is a bipolar-integrated BTSC stereo decoder with hi-fi audio processor (I<sup>2</sup>C-bus controlled) for application in TV sets, VCRs and multimedia.

### Stereo decoder

- Stereo pilot PLL circuit with ceramic resonator, automatic adjustment procedure for stereo channel separation, two pilot thresholds selectable via I<sup>2</sup>C-bus.

### Audio processor

- Selector for internal and external signals (line in)
- Automatic volume level control (control range +6 to -15 dB)
- Interface for external noise reduction circuits
- Volume control (control range +16 to -71 dB)
- Special loudness characteristic automatically controlled in combination with volume setting (control range 28 dB)
- Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- Mute control via I<sup>2</sup>C-bus.

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| TDA9852     | SDIP42  | plastic shrink dual in-line package; 42 leads (600 mil)                          | SOT270-1 |
| TDA9852H    | QFP44   | plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm | SOT307-2 |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## LICENSE INFORMATION

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| COMPANY          | BRANCH               | ADDRESS  |
|------------------|----------------------|--|
| THAT Corporation | Licensing Operations | 734 Forest St.<br>Marlborough, MA 01752<br>USA<br>Tel.: (508) 229-2500<br>Fax: (508) 229-2590                    |
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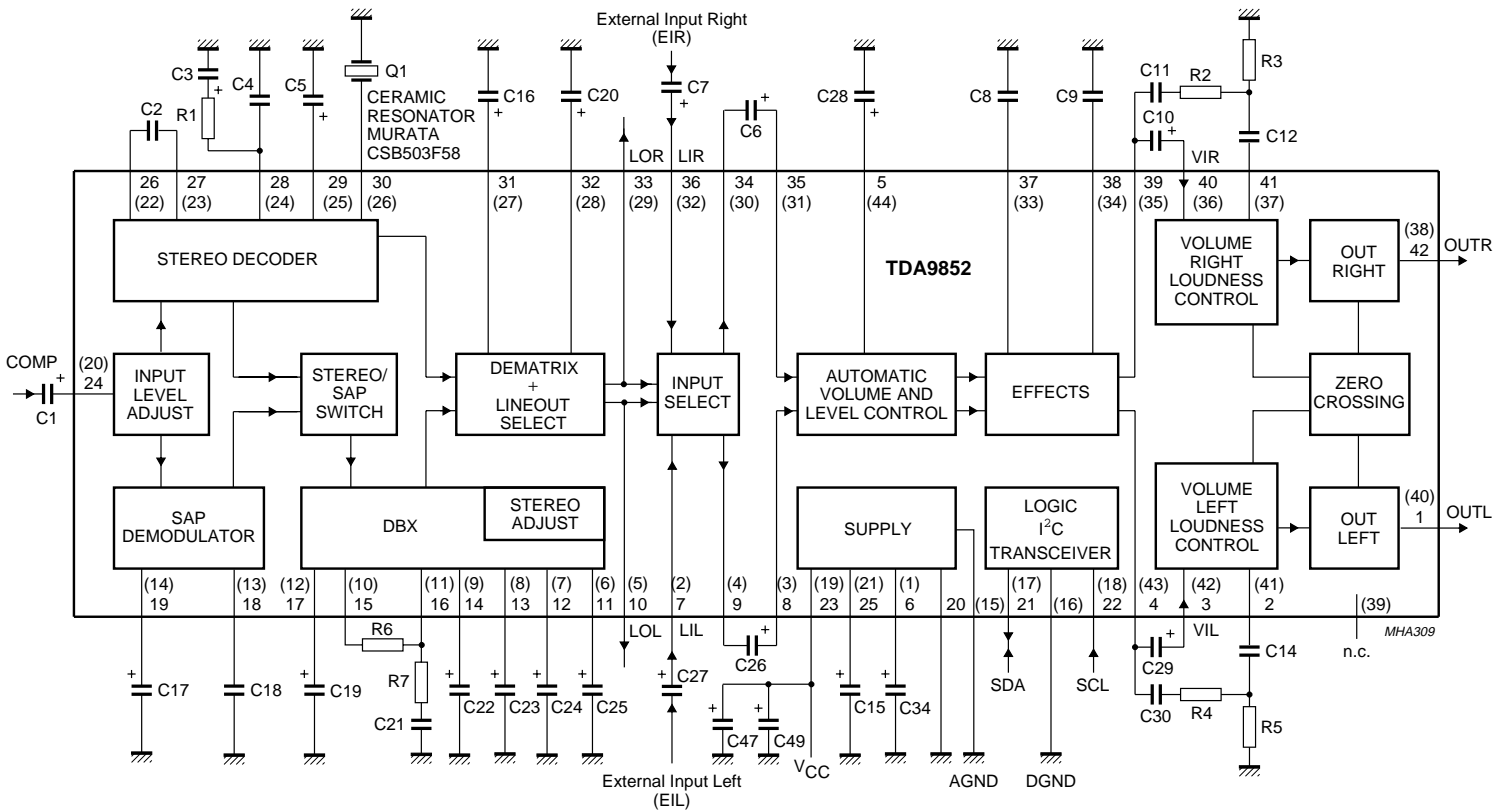
## QUICK REFERENCE DATA

| SYMBOL                 | PARAMETER                         | CONDITIONS   | MIN. | TYP. | MAX. | UNIT |
|------------------------|-----------------------------------|--|------|------|------|------|
| V <sub>CC</sub>        | supply voltage                    |  | 8.0  | 8.5  | 9.0  | V    |
| I <sub>CC</sub>        | supply current                    |  | –    | 75   | 95   | mA   |
| V <sub>comp(rms)</sub> | input signal voltage (RMS value)  | 100% modulation L + R; f <sub>i</sub> = 300 Hz   | –    | 250  | –    | mV   |
| V <sub>oR,L(rms)</sub> | output signal voltage (RMS value) | 100% modulation L + R; f <sub>i</sub> = 300 Hz   | –    | 500  | –    | mV   |
| G <sub>LA</sub>        | input level adjustment control    |  | –3.5 | –    | +4.0 | dB   |
| α <sub>CS</sub>        | stereo channel separation         | f <sub>L</sub> = 300 Hz; f <sub>R</sub> = 3 kHz  | 25   | 35   | –    | dB   |
| THD <sub>L,R</sub>     | total harmonic distortion L + R   | f <sub>i</sub> = 1 kHz   | –    | 0.2  | –    | %    |
| V <sub>I, O(rms)</sub> | signal handling (RMS value)       | THD < 0.5%   | 2    | –    | –    | V    |
| AVL                    | control range                     |  | –15  | –    | +6   | dB   |
| G <sub>C</sub>         | volume control range              |  | –71  | –    | +16  | dB   |
| L <sub>B</sub>         | maximum loudness boost            | f <sub>i</sub> = 40 Hz   | –    | 17   | –    | dB   |
| S/N                    | signal-to-noise ratio             | line out (mono); V <sub>o</sub> = 0.5 V (RMS)<br>CCIR noise weighting filter<br>(peak value)             | –    | 60   | –    | dB   |
|                        |                                   | DIN noise weighting filter<br>(RMS value)  | –    | 73   | –    | dBA  |
| S/N                    | signal-to-noise ratio             | audio section; V <sub>o</sub> = 2 V (RMS);<br>gain = 0 dB<br>CCIR noise weighting filter<br>(peak value) | –    | 94   | –    | dB   |
|                        |                                   | DIN noise weighting filter<br>(RMS value)  | –    | 107  | –    | dBA  |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## BLOCK DIAGRAM



The numbers given in parenthesis refer to the TDA9852H version.

Fig.1 Block diagram.

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

**Component list**Electrolytic capacitors  $\pm 20\%$ ; foil or ceramic capacitors  $\pm 10\%$ ; resistors  $\pm 5\%$ ; unless otherwise specified; see Fig.1.

| COMPONENTS | VALUE          | TYPE            | REMARK                       |
|------------|----------------|-----------------|------------------------------|
| C1         | 10 $\mu$ F     | electrolytic    | 63 V                         |
| C2         | 470 nF         | foil            |                              |
| C3         | 4.7 $\mu$ F    | electrolytic    | 63 V                         |
| C4         | 220 nF         | foil            |                              |
| C5         | 10 $\mu$ F     | electrolytic    | 63 V; $I_{leak} < 1.5 \mu$ A |
| C6         | 2.2 $\mu$ F    | electrolytic    | 16 V                         |
| C7         | 2.2 $\mu$ F    | electrolytic    | 63 V                         |
| C8         | 15 nF          | foil            | $\pm 5\%$                    |
| C9         | 15 nF          | foil            | $\pm 5\%$                    |
| C10        | 2.2 $\mu$ F    | electrolytic    | 16 V                         |
| C11        | 8.2 nF         | foil or ceramic | $\pm 5\%$ SMD 2220/1206      |
| C12        | 150 nF         | foil            | $\pm 5\%$                    |
| C14        | 150 nF         | foil            | $\pm 5\%$                    |
| C15        | 100 $\mu$ F    | electrolytic    | 16 V                         |
| C16        | 4.7 $\mu$ F    | electrolytic    | 63 V                         |
| C17        | 4.7 $\mu$ F    | electrolytic    | 63 V                         |
| C18        | 100 nF         | foil            |                              |
| C19        | 10 $\mu$ F     | electrolytic    | 63 V                         |
| C20        | 4.7 $\mu$ F    | electrolytic    | 63 V                         |
| C21        | 47 nF          | foil            | $\pm 5\%$                    |
| C22        | 1 $\mu$ F      | electrolytic    | 63 V                         |
| C23        | 1 $\mu$ F      | electrolytic    | 63 V                         |
| C24        | 10 $\mu$ F     | electrolytic    | 63 V $\pm 10\%$              |
| C25        | 10 $\mu$ F     | electrolytic    | 63 V $\pm 10\%$              |
| C26        | 2.2 $\mu$ F    | electrolytic    | 16 V                         |
| C27        | 2.2 $\mu$ F    | electrolytic    | 63 V                         |
| C28        | 4.7 $\mu$ F    | electrolytic    | 63 V $\pm 10\%$              |
| C29        | 2.2 $\mu$ F    | electrolytic    | 16 V                         |
| C30        | 8.2 nF         | foil or ceramic | $\pm 5\%$ SMD 2220/1206      |
| C34        | 100 $\mu$ F    | electrolytic    | 16 V                         |
| C47        | 220 $\mu$ F    | electrolytic    | 25 V                         |
| C49        | 100 nF         | foil or ceramic | SMD 1206                     |
| R1         | 2.2 k $\Omega$ | –               |                              |
| R2         | 20 k $\Omega$  | –               |                              |
| R3         | 2.2 k $\Omega$ | –               |                              |
| R4         | 20 k $\Omega$  | –               |                              |
| R5         | 2.2 k $\Omega$ | –               |                              |
| R6         | 8.2 k $\Omega$ | –               | $\pm 2\%$                    |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| COMPONENTS | VALUE        | TYPE        | REMARK             |
|------------|--------------|-------------|--------------------|
| R7         | 160 $\Omega$ | –           | $\pm 2\%$          |
| Q1         |              | CSB503F58   | radial leads       |
|            |              | CSB503JF958 | alternative as SMD |

## PINNING

| SYMBOL           | PINS   |       | DESCRIPTION                                     |
|------------------|--------|-------|---|
|                  | SDIP42 | QFP44 |   |
| OUTL             | 1      | 40    | output, left channel                            |
| LDL              | 2      | 41    | input loudness, left channel                    |
| VIL              | 3      | 42    | input volume, left channel                      |
| EOL              | 4      | 43    | output effects, left channel                    |
| C <sub>AV</sub>  | 5      | 44    | automatic volume control capacitor              |
| V <sub>ref</sub> | 6      | 1     | reference voltage 0.5V <sub>CC</sub>            |
| LIL              | 7      | 2     | input line control, left channel                |
| AVL              | 8      | 3     | input automatic volume control, left channel    |
| SOL              | 9      | 4     | output selector, left channel                   |
| LOL              | 10     | 5     | output line control, left channel               |
| C <sub>TW</sub>  | 11     | 6     | capacitor timing wideband for dbx               |
| C <sub>TS</sub>  | 12     | 7     | capacitor timing spectral for dbx               |
| C <sub>W</sub>   | 13     | 8     | capacitor wideband for dbx                      |
| C <sub>S</sub>   | 14     | 9     | capacitor spectral for dbx                      |
| VEO              | 15     | 10    | variable emphasis output for dbx                |
| VEI              | 16     | 11    | variable emphasis input for dbx                 |
| C <sub>NR</sub>  | 17     | 12    | capacitor noise reduction for dbx               |
| C <sub>M</sub>   | 18     | 13    | capacitor mute for SAP                          |
| C <sub>DEC</sub> | 19     | 14    | capacitor DC-decoupling for SAP                 |
| GND              | 20     | –     | ground  |
| AGND             | –      | 15    | analog ground                                   |
| DGND             | –      | 16    | digital ground                                  |
| SDA              | 21     | 17    | serial data input/output (I <sup>2</sup> C-bus) |
| SCL              | 22     | 18    | serial clock input (I <sup>2</sup> C-bus)       |
| V <sub>CC</sub>  | 23     | 19    | supply voltage                                  |
| COMP             | 24     | 20    | composite input signal                          |
| V <sub>CAP</sub> | 25     | 21    | capacitor for electronic filtering of supply    |
| C <sub>P1</sub>  | 26     | 22    | capacitor for pilot detector                    |
| C <sub>P2</sub>  | 27     | 23    | capacitor for pilot detector                    |
| C <sub>PH</sub>  | 28     | 24    | capacitor for phase detector                    |
| C <sub>ADJ</sub> | 29     | 25    | capacitor for filter adjustment                 |
| CER              | 30     | 26    | ceramic resonator                               |
| C <sub>MO</sub>  | 31     | 27    | capacitor DC-decoupling mono                    |

I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| SYMBOL           | PINS   |       | DESCRIPTION                                   |
|------------------|--------|-------|---|
|                  | SDIP42 | QFP44 |   |
| C <sub>SS</sub>  | 32     | 28    | capacitor DC-decoupling stereo/SAP            |
| LOR              | 33     | 29    | output line control, right channel            |
| SOR              | 34     | 30    | output selector, right channel                |
| AVR              | 35     | 31    | input automatic volume control, right channel |
| LIR              | 36     | 32    | input line control, right channel             |
| C <sub>PS2</sub> | 37     | 33    | capacitor 2 pseudo function                   |
| C <sub>PS1</sub> | 38     | 34    | capacitor 1 pseudo function                   |
| EOR              | 39     | 35    | output effects, right channel                 |
| VIR              | 40     | 36    | input volume, right channel                   |
| LDR              | 41     | 37    | input loudness, right channel                 |
| OUTR             | 42     | 38    | output, right channel                         |
| n.c.             | –      | 39    | not connected                                 |

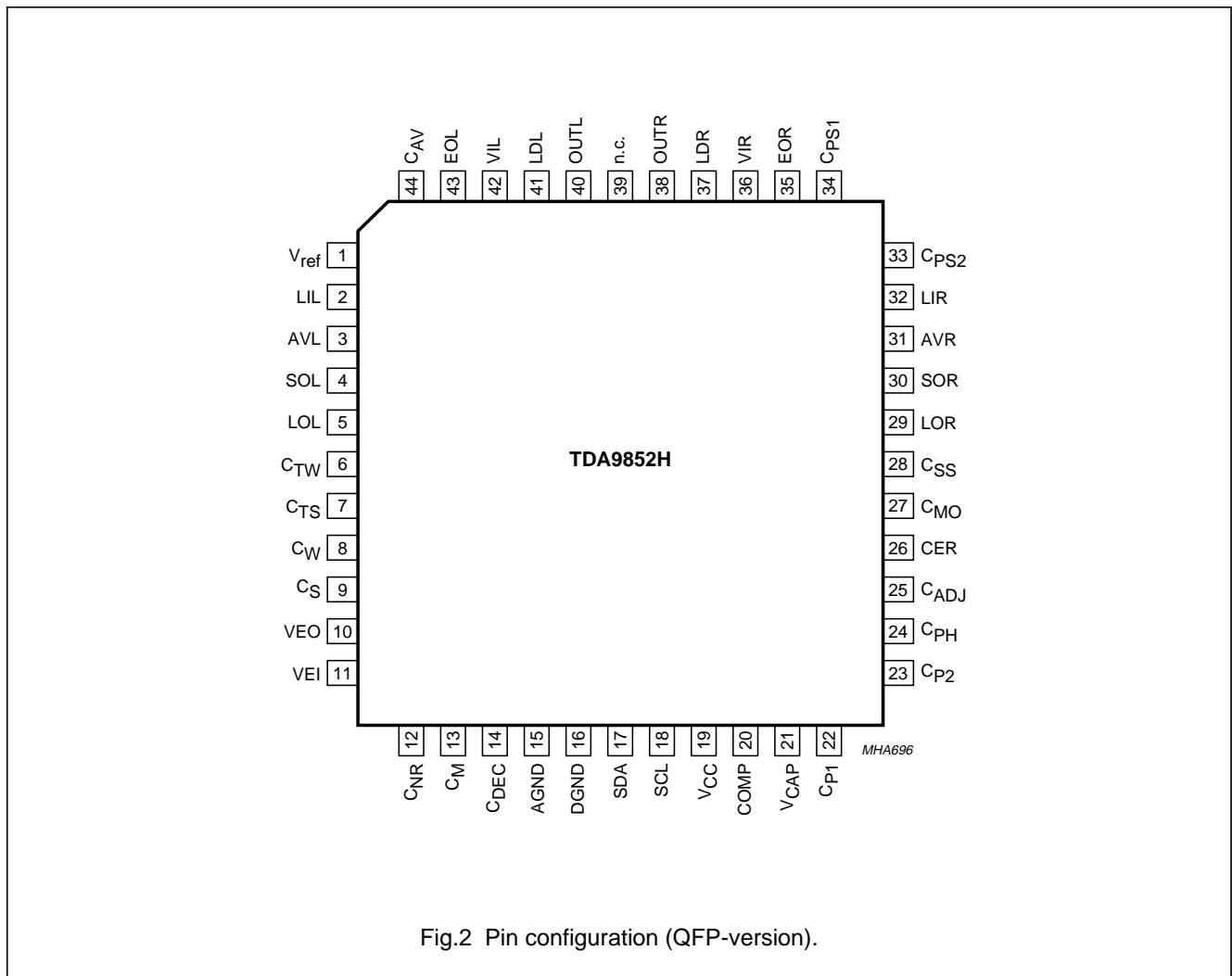


Fig.2 Pin configuration (QFP-version).

I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

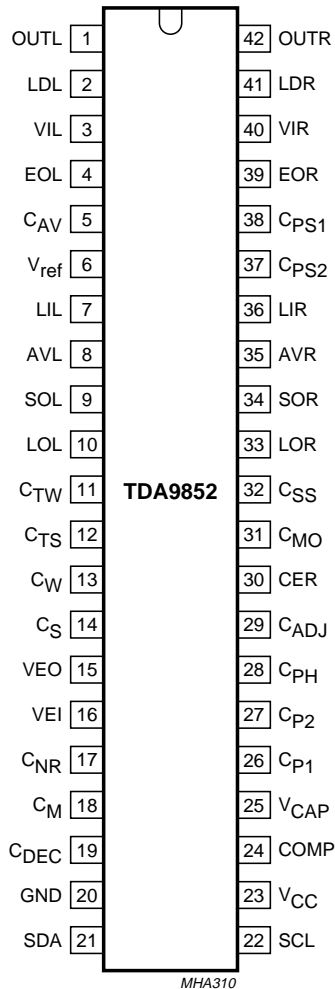


Fig.3 Pin configuration (SDIP-version).

FUNCTIONAL DESCRIPTION

Stereo decoder

INPUT LEVEL ADJUSTMENT

The composite input signal is fed to the input level adjustment stage. The control range is from -3.5 to +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 5 and 6 and the level adjust setting of Table 21 allows an optimum signal adjustment during the set alignment. The maximum input signal voltage is 2 V (RMS).

STEREO DECODER

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 μs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded sub-signal L - R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation is adjusted by an automatic procedure to be performed during set production. For a detailed description see Section "Adjustment procedure". The stereo identification can be read by the I<sup>2</sup>C-bus (see Table 2). Two different pilot thresholds (data STS = 1; STS = 0) can be selected via the I<sup>2</sup>C-bus (see Table 19).

SAP DEMODULATOR

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a 5f<sub>H</sub> (f<sub>H</sub> = horizontal frequency) band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in the event of insufficient signal conditions. The SAP identification signal can be read by the I<sup>2</sup>C-bus (see Table 2).

SWITCH

The stereo/SAP switch feeds either the L - R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/switching circuit. Table 12 shows the different switch modes provided at the output pins LOR and LOL.



## I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

### dbx DECODER

The circuit includes all blocks required for the noise reduction system in accordance with the BTSC system specification. The output signal is fed through a 73  $\mu$ s fixed de-emphasis circuit to the dematrix block.

### INTEGRATED FILTERS

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on-chip using transistor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

### Audio processor

#### SELECTOR

The selector allows selecting either the internal line out signals LOR or LOL (dematrix output) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Tables 5 and 6 for subaddress and Table 11 for data). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS). The output of the selector is AC-coupled to the automatic volume level control circuit via pins SOR/SOL and AVR/AVL to avoid offset voltages.

#### AUTOMATIC VOLUME LEVEL CONTROL

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range of 0.1 to 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and due to changes in the programme material. The function can be switched **off**. To avoid audible 'plops' during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor (4.7  $\mu$ F) at pin C<sub>AV</sub> determines the attack and decay time constants. In addition the ratio of attack and decay time can be changed via I<sup>2</sup>C-bus (see Table 15). At power **on**, the discharged 4.7  $\mu$ F capacitor at C<sub>AV</sub> must be loaded by the internal decay current. If AVL is chosen, this would result in an attenuated AVL gain for about 10 seconds after power **on**. This can be speeded up by choosing via I<sup>2</sup>C-bus an increased charge current (about 10 times higher) for about the first 2 seconds after power **on** (see Table 6, CCD bit in control 1 and Table 18).

### EFFECTS

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono. The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via I<sup>2</sup>C-bus; see Table 10).

### VOLUME/LOUDNESS

The volume control range is from +16 dB to -71 dB in steps of 1 dB and ends with a mute step (see Table 8). Balance control is achieved by the independent volume control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of -12 dB. At -12 dB volume control the maximum loudness boost is obtained. The filter characteristic is determined by external components. The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched **on** or **off** via I<sup>2</sup>C-bus control (see Table 9). The left and right volume control stages include two independent zero crossing detectors. A change in volume is automatically activated but not executed. The execution is enabled at the next zero crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero crossing occurs the next volume transmission will enforce the last activated volume setting.

The zero crossing is realized between adjoining steps and between any steps, but not from any step to mute. In this case the GMU bit is needed to use. In case only one channel has to be muted, two steps are necessary. The first step is a transmission of any step to -71 dB and the second step is the -71 dB step to mute mode. The step of -71 dB to mute mode has no zero crossing but this is not relevant.

## I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

### MUTE

The mute function can be activated independently with last step of volume control at the left or right output. By setting the general mute bit GMU via the I<sup>2</sup>C-bus all outputs are muted. All channels include an independent zero cross detector. The zero crossing mute feature can be selected via bit TZCM:

TZCM = 0: forced mute with direct execution

TZCM = 1: execution in time with signal zero crossing.

In the zero cross mode a change in the GMU polarity is activated but not executed. The execution is enabled at the next zero crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I<sup>2</sup>C-bus transmissions are needed:

a first transmission for mute execution

a second transmission about 100 ms later, which must switch the zero crossing mode to forced mute (TZCM = 0)

a third transmission to reactivate the zero crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

### Adjustment procedure

#### COMPOSITE INPUT LEVEL ADJUSTMENT

Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R;  $f_i = 300$  Hz. Set input level control via I<sup>2</sup>C-bus monitoring line out (500 mV  $\pm$ 20 mV). Store the setting in a non-volatile memory.

#### AUTOMATIC ADJUSTMENT PROCEDURE

- Capacitors of external inputs LIL and LIR must be grounded at EIL and EIR
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via I<sup>2</sup>C-bus

- Effects, AVL, loudness **off**.
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 12)
- Selector setting SC0, SC1, SC2 = 0, 0, 0 (see Table 11)
- Start adjustment by transmission ADJ = 1 in register ALI3; the decoder will align itself
- After 1 second minimum stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I<sup>2</sup>C-bus read operation from ALR1 and ALR2 (see Chapter "I<sup>2</sup>C-bus protocol") and store it in a non-volatile memory; the alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

#### MANUAL ADJUSTMENT

Manual adjustment is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz; 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz; 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimum adjustment
- Store data in non-volatile memory.

#### TIMING CURRENT FOR RELEASE RATE

Due to possible internal and external spreading, the timing current can be adjusted via I<sup>2</sup>C-bus, see Table 20, as recommended by dbx.

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## Requirements for the composite input signal to ensure correct system performance

| SYMBOL                   | PARAMETER   | CONDITIONS   | MIN. | TYP.      | MAX. | UNIT |
|--------------------------|---|--|------|-----------|------|------|
| COMP <sub>L+R(rms)</sub> | composite input level for 100% modulation L + R; 25 kHz deviation; f <sub>i</sub> = 300 Hz; RMS value | measured at COMP   | 162  | 250       | 363  | mV   |
| ΔCOMP                    | composite input level spreading under operating conditions  | T <sub>amb</sub> = -20 to +70 °C; aging; power supply influence  | -0.5 | -         | +0.5 | dB   |
| Z <sub>o</sub>           | output impedance  | note 1   | -    | low-ohmic | 5    | kΩ   |
| f <sub>lf</sub>          | low frequency roll-off  | 25 kHz deviation L + R; -2 dB  | -    | -         | 5    | Hz   |
| f <sub>hf</sub>          | high frequency roll-off   | 25 kHz deviation L + R; -2 dB  | 100  | -         | -    | kHz  |
| THD <sub>L,R</sub>       | total harmonic distortion L + R   | f <sub>i</sub> = 1 kHz; 25 kHz deviation   | -    | -         | 0.5  | %    |
|                          |   | f <sub>i</sub> = 1 kHz; 125 kHz deviation; note 2  | -    | -         | 1.5  | %    |
| S/N                      | signal-to-noise ratio L + R/noise   | CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f <sub>i</sub> = 1 kHz; 75 μs de-emphasis critical picture modulation; note 3 | 44   | -         | -    | dB   |
|                          |   | with sync only   | 54   | -         | -    | dB   |
| α <sub>SB</sub>          | side band suppression mono into unmodulated SAP carrier; SAP carrier/side band                        | mono signal: 25 kHz deviation, f <sub>i</sub> = 1 kHz; side band: SAP carrier frequency ±1 kHz   | 46   | -         | -    | dB   |
| α <sub>SP</sub>          | spectral spurious attenuation L + R/spurious  | 50 Hz to 100 kHz; mainly n × f <sub>H</sub> ; no de-emphasis; L + R; 25 kHz deviation, f = 1 kHz as reference                          |      |           |      |      |
|                          |   | n = 1, 5   | 35   | -         | -    | dB   |
|                          |   | n = 4, 6   | 40   | -         | -    | dB   |
|                          |   | n = 2, 3   | 26   | -         | -    | dB   |

### Notes

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z<sub>o</sub> and the composite input impedance (see Chapter "Characteristics", Section "Input level adjustment control") must be taken into account.
2. In order to prevent clipping at over-modulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).
3. For example colour bar or flat field white; 100% video modulation.

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL           | PARAMETER  | MIN. | MAX.            | UNIT |
|------------------|--|------|-----------------|------|
| V <sub>CC</sub>  | supply voltage                                   | 0    | 9.5             | V    |
| V <sub>n</sub>   | voltage of all other pins to pin V <sub>CC</sub> | 0    | V <sub>CC</sub> | V    |
| T <sub>amb</sub> | operating ambient temperature                    | -20  | +70             | °C   |
| T <sub>stg</sub> | storage temperature                              | -65  | +150            | °C   |
| V <sub>es</sub>  | electrostatic handling; note 1                   |      |                 |      |

### Note

- Human body model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; Charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

## THERMAL CHARACTERISTICS

| SYMBOL              | PARAMETER   | VALUE | UNIT |
|---------------------|---|-------|------|
| R <sub>th j-a</sub> | thermal resistance from junction to ambient in free air |       |      |
|                     | SOT270-1  | 43    | K/W  |
|                     | SOT307-2  | 60    | K/W  |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## CHARACTERISTICS

All voltages are measured relative to GND;  $V_{CC} = 8.5$  V;  $R_s = 600$   $\Omega$ ;  $R_L = 10$  k $\Omega$ ;  $C_L = 2.5$  nF; AC-coupled;  $f_i = 1$  kHz;  $T_{amb} = 25$  °C; gain control  $G_v = 0$  dB; balance in mid position; loudness **off**; see Fig.1; unless otherwise specified.

| SYMBOL                                | PARAMETER  | CONDITIONS   | MIN. | TYP. | MAX. | UNIT       |
|---------------------------------------|--|--|------|------|------|------------|
| <b>General</b>                        |  |  |      |      |      |            |
| $V_{CC}$                              | supply voltage   |  | 8.0  | 8.5  | 9.0  | V          |
| $I_{CC}$                              | supply current   |  | –    | 75   | 95   | mA         |
| $V_{ref}$                             | internal reference voltage at pin $V_{ref}$                                  |  | –    | 4.25 | –    | V          |
| <b>Input level adjustment control</b> |  |  |      |      |      |            |
| $G_{LA}$                              | input level adjustment control   |  | –3.5 | –    | +4.0 | dB         |
| $G_{step}$                            | step resolution  |  | –    | 0.5  | –    | dB         |
| $V_{i(rms)}$                          | maximum input voltage level (RMS value)                                      |  | 2    | –    | –    | V          |
| $Z_i$                                 | input impedance  |  | 29.5 | 35   | 40.5 | k $\Omega$ |
| <b>Stereo decoder</b>                 |  |  |      |      |      |            |
| $MPX_{L+R(rms)}$                      | input voltage level for 100% modulation L + R; 25 kHz deviation (RMS value)  | input level adjusted via I <sup>2</sup> C-bus (L + R; $f_i = 300$ Hz); monitoring LINE OUT                                     | –    | 250  | –    | mV         |
| $MPX_{L-R}$                           | input voltage level for 100% modulation L – R; 50 kHz deviation (peak value) |  | –    | 707  | –    | mV         |
| $MPX_{(max)}$                         | maximum headroom for L + R, L, R   | $f_{mod} < 15$ kHz; THD < 15%  | 9    | –    | –    | dB         |
| $MPX_{pilot(rms)}$                    | nominal stereo pilot voltage level (RMS value)                               |  | –    | 50   | –    | mV         |
| $ST_{on(rms)}$                        | pilot threshold voltage stereo <b>on</b> (RMS value)                         | data STS = 1   | –    | –    | 35   | mV         |
|                                       |  | data STS = 0   | –    | –    | 30   | mV         |
| $ST_{off(rms)}$                       | pilot threshold voltage stereo <b>off</b> (RMS value)                        | data STS = 1   | 15   | –    | –    | mV         |
|                                       |  | data STS = 0   | 10   | –    | –    | mV         |
| $Hys$                                 | hysteresis   |  | –    | 2.5  | –    | dB         |
| $OUT_{L+R}$                           | output voltage level for 100% modulation L + R at LINE OUT                   | input level adjusted via I <sup>2</sup> C-bus (L + R; $f_i = 300$ Hz); monitoring LINE OUT                                     | 480  | 500  | 520  | mV         |
| $\alpha_{cs}$                         | stereo channel separation L/R at LINE OUT                                    | aligned with dual tone 14% modulation for each channel; see Section “Adjustment procedure” in Chapter “Functional description” |      |      |      |            |
|                                       |  | $f_L = 300$ Hz; $f_R = 3$ kHz  | 25   | 35   | –    | dB         |
|                                       |  | $f_L = 300$ Hz; $f_R = 8$ kHz  | 20   | 30   | –    | dB         |
|                                       |  | $f_L = 300$ Hz; $f_R = 10$ kHz   | 15   | 25   | –    | dB         |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| SYMBOL   | PARAMETER   | CONDITIONS  | MIN.      | TYP.      | MAX.   | UNIT     |
|--|---|---|-----------|-----------|--------|----------|
| $f_{L,R}$  | L, R frequency response                             | 14% modulation;<br>$f_{ref} = 300$ Hz L or R<br>$f_i = 50$ Hz to 10 kHz<br>$f_i = 12$ kHz | -3<br>-   | -<br>-3   | -<br>- | dB<br>dB |
| THD <sub>L,R</sub>                               | total harmonic distortion L, R at LINE OUT          | modulation L or R<br>1% to 100%; $f_i = 1$ kHz  | -         | 0.2       | 1.0    | %        |
| S/N  | signal-to-noise ratio                               | mono mode; CCIR 468-2 weighted; quasi peak; 500 mV output signal                          | 50        | 60        | -      | dB       |
| <b>Stereo decoder, oscillator (VCXO); note 1</b> |   |   |           |           |        |          |
| $f_o$  | nominal VCXO output frequency ( $32f_H$ )           | with nominal ceramic resonator  | -         | 503.5     | -      | kHz      |
| $f_{of}$   | spread of free-running frequency                    | with nominal ceramic resonator  | 500.0     | -         | 507.0  | kHz      |
| $\Delta f_H$                                     | capture range frequency (nominal pilot)             |   | $\pm 190$ | $\pm 265$ | -      | Hz       |
| <b>SAP demodulator; note 2</b>                   |   |   |           |           |        |          |
| SAP <sub>i(rms)</sub>                            | nominal SAP carrier input voltage level (RMS value) | 15 kHz frequency deviation of intercarrier  | -         | 150       | -      | mV       |
| SAP <sub>on(rms)</sub>                           | threshold voltage SAP on (RMS value)                |   | -         | -         | 85     | mV       |
| SAP <sub>off(rms)</sub>                          | threshold voltage SAP off (RMS value)               |   | 35        | -         | -      | mV       |
| SAP <sub>hys</sub>                               | hysteresis  |   | -         | 2         | -      | dB       |
| SAP <sub>LEV</sub>                               | SAP output voltage level at LINE OUT                | mode selector in position SAP/SAP; $f_{mod} = 300$ Hz; 100% modulation                    | -         | 500       | -      | mV       |
| $f_{res}$  | frequency response                                  | 14% modulation; 50 Hz to 8 kHz; $f_{ref} = 300$ Hz  | -3        | -         | -      | dB       |
| THD  | total harmonic distortion                           | $f_i = 1$ kHz   | -         | 0.5       | 2.0    | %        |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| SYMBOL                              | PARAMETER  | CONDITIONS  | MIN.                | TYP.               | MAX.                | UNIT |
|-------------------------------------|--|---|---------------------|--------------------|---------------------|------|
| <b>LINE OUT at pins LOL and LOR</b> |  |   |                     |                    |                     |      |
| $V_{o(rms)}$                        | nominal output voltage (RMS value)                                       | 100% modulation   | –                   | 500                | –                   | mV   |
| HEAD <sub>o</sub>                   | output headroom  |   | 9                   | –                  | –                   | dB   |
| Z <sub>o</sub>                      | output impedance   |   | –                   | 80                 | 120                 | Ω    |
| V <sub>O</sub>                      | DC output voltage  |   | 0.45V <sub>CC</sub> | 0.5V <sub>CC</sub> | 0.55V <sub>CC</sub> | V    |
| R <sub>L</sub>                      | output load resistance   |   | 5                   | –                  | –                   | kΩ   |
| C <sub>L</sub>                      | output load capacitance  |   | –                   | –                  | 2.5                 | nF   |
| $\alpha_{ct}$                       | crosstalk L, R into SAP  | 100% modulation; f <sub>i</sub> = 1 kHz; L or R; mode selector switched to SAP/SAP                            | 50                  | 75                 | –                   | dB   |
|                                     | crosstalk SAP into L, R  | 100% modulation; f <sub>i</sub> = 1 kHz; SAP; mode selector switched to stereo                                | 50                  | 70                 | –                   | dB   |
| $\Delta V_{ST-SAP}$                 | output voltage difference if switched from L, R to SAP                   | 250 Hz to 6.3 kHz   | –                   | –                  | 3                   | dB   |
| <b>dbx noise reduction circuit</b>  |  |   |                     |                    |                     |      |
| t <sub>adj</sub>                    | stereo adjustment time   | see Section "Adjustment procedure" in Chapter "Functional description"  | –                   | –                  | 1                   | s    |
| I <sub>s</sub>                      | nominal timing current for nominal release rate of spectral RMS detector | I <sub>s</sub> can be measured at pin C <sub>TS</sub> via current meter connected to 1/2V <sub>CC</sub> + 1 V | –                   | 24                 | –                   | μA   |
| ΔI <sub>s</sub>                     | spread of timing current   |   | –15                 | –                  | +15                 | %    |
| I <sub>s range</sub>                | timing current range   | 7 steps via I <sup>2</sup> C-bus  | –                   | ±30                | –                   | %    |
| I <sub>t</sub>                      | timing current for release rate of wideband RMS detector                 |   | –                   | 1/3I <sub>s</sub>  | –                   | μA   |
| Rel <sub>rate</sub>                 | nominal RMS detector release rate  | nominal timing current and external capacitor values  |                     |                    |                     |      |
|                                     |  | wideband  | –                   | 125                | –                   | dB/s |
|                                     | spectral   | –   | 381                 | –                  | dB/s                |      |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| SYMBOL   | PARAMETER  | CONDITIONS   | MIN.    | TYP.   | MAX.    | UNIT          |
|--|--|--|---------|--------|---------|---------------|
| <b>Circuit section from pins LIL and LIR to pins OUTL and OUTR; note 3</b> |  |  |         |        |         |               |
| B  | roll-off frequencies                               | $C_6, C_7, C_{10}, C_{26}, C_{27}$ and<br>$C_{29} = 2.2 \mu\text{F}; Z_i = Z_{i(\text{min})}$<br>low frequency (-3 dB)<br>high frequency (-0.5 dB) | -<br>20 | -<br>- | 20<br>- | Hz<br>kHz     |
| THD  | total harmonic distortion                          | $V_i = 1000 \text{ mV}; G_v = 0 \text{ dB};$<br>AVL <b>on</b>  | -       | 0.2    | 0.5     | %             |
|  |  | $V_i = 2000 \text{ mV}; G_v = 0 \text{ dB};$<br>AVL <b>on</b>  | -       | 0.2    | 0.5     | %             |
|  |  | $V_i = 1000 \text{ mV}; G_v = 0 \text{ dB};$<br>AVL <b>off</b>   | -       | 0.02   | -       | %             |
|  |  | $V_i = 2000 \text{ mV}; G_v = 0 \text{ dB};$<br>AVL <b>off</b>   | -       | 0.02   | -       | %             |
| RR   | ripple rejection                                   | $V_{r(\text{rms})} < 200 \text{ mV}; f_i = 100 \text{ Hz}$   | 47      | 50     | -       | dB            |
| $\alpha_{\text{ct}}$   | crosstalk between bus inputs<br>and signal outputs | notes 4 and 5  | -       | 110    | -       | dB            |
| $V_{\text{no}}$  | noise output voltage                               | CCIR 468-2 weighted; quasi<br>peak; AVL <b>off</b> ; loudness <b>off</b> ;<br>$G_v = 0 \text{ dB}$   | -       | 40     | 80      | $\mu\text{V}$ |
|  |  | measured in dBA; AVL <b>off</b> ;<br>loudness <b>off</b> ; $G_v = 0 \text{ dB}$  | -       | 8      | -       | $\mu\text{V}$ |
| $\alpha_{\text{cs}}$   | channel separation                                 | $V_i = 1 \text{ V}; f_i = 1 \text{ kHz}$   | 75      | -      | -       | dB            |
|  |  | $V_i = 1 \text{ V}; f_i = 12.5 \text{ kHz}$  | 75      | -      | -       | dB            |
| <b>Effect controls</b>   |  |  |         |        |         |               |
| $\alpha_{\text{spat1}}$  | anti-phase crosstalk by spatial<br>effect          |  | -       | 52     | -       | %             |
| $\alpha_{\text{spat2}}$  |  |  | -       | 30     | -       | %             |
| $\varphi$  | phase shift by pseudo-stereo                       | see Fig.4  | -       | -      | -       | -             |



# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| SYMBOL  | PARAMETER  | CONDITIONS  | MIN. | TYP.  | MAX. | UNIT |
|---|--|---|------|-------|------|------|
| <b>Automatic volume level control (AVL)</b>                         |  |   |      |       |      |      |
| Z <sub>i</sub>  | input impedance  |   | 8.8  | 11.0  | 13.2 | kΩ   |
| V <sub>i(rms)</sub>   | maximum input voltage (RMS value)                                      | THD < 0.2%  | 2    | tbf   | –    | V    |
| G <sub>v</sub>  | gain, maximum boost  |   | 5    | 6     | 7    | dB   |
|   | maximum attenuation  |   | 14   | 15    | 16   | dB   |
| G <sub>step</sub>   | equivalent step width between the input stages (soft switching system) |   | –    | 1.5   | –    | dB   |
| V <sub>iop(rms)</sub>   | input level at maximum boost (RMS value)                               |   | –    | 0.1   | –    | V    |
|   | input level at maximum attenuation (RMS value)                         |   | –    | 1.125 | –    | V    |
| V <sub>o(rms)</sub>   | output level in AVL operation (RMS value)                              | see Fig.5   | 160  | 200   | 250  | mV   |
| V <sub>DC OFF</sub>   | DC offset between different gain steps                                 | voltage at pin C <sub>AV</sub><br>6.50 to 6.33 V or<br>6.33 to 6.11 V or<br>6.11 to 5.33 V or<br>5.33 to 2.60 V; note 6 | –    | –     | 6    | mV   |
| R <sub>att</sub>  | discharge resistors for attack time constant                           | AT1 = 0; AT2 = 0; note 7  | 340  | 420   | 520  | Ω    |
|   |  | AT1 = 1; AT2 = 0; note 7  | 590  | 730   | 910  | Ω    |
|   |  | AT1 = 0; AT2 = 1; note 7  | 0.96 | 1.2   | 1.5  | kΩ   |
|   |  | AT1 = 1; AT2 = 1; note 7  | 1.7  | 2.1   | 2.6  | kΩ   |
| I <sub>dec</sub>  | charge current for decay time  | normal mode; CCD = 0; note 8  | 1.6  | 2.0   | 2.4  | μA   |
|   |  | power-on speed-up; CCD = 1; note 8  | –    | tbf   | –    | μA   |
| <b>Selector from pins LOL, LOR, LIL and LIR to pins SOL and SOR</b> |  |   |      |       |      |      |
| Z <sub>i</sub>  | input impedance  |   | 16   | 20    | 24   | kΩ   |
| α <sub>s</sub>  | input isolation of one selected source to the other input              | V <sub>i</sub> = 1 V; f <sub>i</sub> = 1 kHz  | 86   | 96    | –    | dB   |
|   |  | V <sub>i</sub> = 1 V; f <sub>i</sub> = 12.5 kHz   | 80   | 96    | –    | dB   |
| V <sub>i(rms)</sub>   | maximum input voltage (RMS value)                                      | THD < 0.5%  | 2    | 2.3   | –    | V    |
| V <sub>DC OFF</sub>   | DC offset voltage at selector output by selection of any inputs        |   | –    | –     | 25   | mV   |
| Z <sub>o</sub>  | output impedance   |   | –    | 80    | 120  | Ω    |
| R <sub>L</sub>  | output load resistance   |   | 5    | –     | –    | kΩ   |
| C <sub>L</sub>  | output load capacitance  |   | 0    | –     | 2.5  | nF   |
| G <sub>v</sub>  | voltage gain, selector   |   | –    | 0     | –    | dB   |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| SYMBOL  | PARAMETER                                   | CONDITIONS  | MIN. | TYP.                   | MAX.           | UNIT           |
|---|---|---|------|------------------------|----------------|----------------|
| <b>Audio control part; input pins VIL and VIR to pins OUTX and OUTS</b> |   |   |      |                        |                |                |
| Z <sub>i</sub>  | volume input impedance                      |   | 8.0  | 10.0                   | 12.0           | kΩ             |
| Z <sub>o</sub>  | output impedance                            |   | –    | 80                     | 120            | Ω              |
| R <sub>L</sub>  | output load resistance                      |   | 5    | –                      | –              | kΩ             |
| C <sub>L</sub>  | output load capacitance                     |   | 0    | –                      | 2.5            | nF             |
| V <sub>i(rms)</sub>   | maximum input voltage<br>(RMS value)        | THD < 0.5%  | 2.0  | 2.15                   | –              | V              |
| V <sub>no</sub>   | noise output voltage                        | CCIR 468-2 weighted;<br>quasi peak<br>G <sub>v</sub> = 16 dB<br>G <sub>v</sub> = 0 dB<br>mute position  | –    | 110<br>33<br>10        | 220<br>50<br>– | μV<br>μV<br>μV |
| G <sub>c</sub>  | total continuous control range              | maximum boost   | –    | 16                     | –              | dB             |
|   |   | maximum attenuation   | –    | 71                     | –              | dB             |
| G <sub>step</sub>   | step resolution                             |   | –    | 1                      | –              | dB             |
|   | step error between adjoining<br>step        |   | –    | –                      | 0.5            | dB             |
| ΔG <sub>a</sub>   | attenuator set error                        | G <sub>v</sub> = +16 to –50 dB  | –    | –                      | 2              | dB             |
|   |   | G <sub>v</sub> = –51 to –71 dB  | –    | –                      | 3              | dB             |
| ΔG <sub>L</sub>   | gain tracking error                         | G <sub>v</sub> = +16 to –50 dB  | –    | –                      | 2              | dB             |
| α <sub>m</sub>  | mute attenuation                            |   | 80   | –                      | –              | dB             |
| V <sub>DC OFF</sub>   | DC step offset between any<br>adjacent step | G <sub>v</sub> = +16 to 0 dB  | –    | 0.2                    | 10.0           | mV             |
|   |   | G <sub>v</sub> = 0 to –71 dB  | –    | –                      | 5              | mV             |
|   | DC step offset between any<br>step to mute  | G <sub>v</sub> = +16 to +1 dB   | –    | 2                      | 15             | mV             |
|   |   | G <sub>v</sub> = 0 to –71 dB  | –    | 1                      | 10             | mV             |
| <b>Loudness control part</b>  |   |   |      |                        |                |                |
| L <sub>B</sub>  | maximum loudness boost                      | loudness <b>on</b> ; referred to<br>loudness <b>off</b> ; boost is<br>determined by external<br>components; see Fig.6<br>f <sub>i</sub> = 40 Hz | –    | 17                     | –              | dB             |
|   |   | f <sub>i</sub> = 10 kHz   | –    | 4.5                    | –              | dB             |
| L <sub>G</sub>  | loudness control range                      |   | –12  | –                      | +16            |                |
| <b>Muting at power supply drop for OUTR and OUTS</b>                    |   |   |      |                        |                |                |
| V <sub>CC-DROP</sub>  | supply drop for mute active                 |   | –    | V <sub>CAP</sub> – 0.7 | –              | V              |
| <b>Power-on reset; note 9</b>   |   |   |      |                        |                |                |
| V <sub>RESET(STA)</sub>   | start of reset voltage                      | increasing supply voltage   | –    | –                      | 2.5            | V              |
|   |   | decreasing supply voltage   | 4.2  | 5                      | 5.8            | V              |
| V <sub>RESET(END)</sub>   | end of reset voltage                        | increasing supply voltage   | 5.2  | 6                      | 6.8            | V              |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| SYMBOL   | PARAMETER                | CONDITIONS            | MIN. | TYP. | MAX.            | UNIT |
|--|--------------------------|-----------------------|------|------|-----------------|------|
| <b>Digital part (I<sup>2</sup>C-bus pins); note 10</b> |                          |                       |      |      |                 |      |
| V <sub>IH</sub>  | HIGH level input voltage |                       | 3    | –    | V <sub>CC</sub> | V    |
| V <sub>IL</sub>  | LOW level input voltage  |                       | –0.3 | –    | +1.5            | V    |
| I <sub>IH</sub>  | HIGH level input current |                       | –10  | –    | +10             | μA   |
| I <sub>IL</sub>  | LOW level input current  |                       | –10  | –    | +10             | μA   |
| V <sub>OL</sub>  | LOW level output voltage | I <sub>L</sub> = 3 mA | –    | –    | +0.4            | V    |

### Notes to the characteristics

- The oscillator is designed to operate together with MURATA resonator CSB503F58. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58.
- The internal SAP carrier level is determined by the composite input level and the level adjustment gain.
- Frequency range 20 Hz to 20 kHz; select in to input line control; effects: linear stereo.

- Crosstalk:  $20 \log \frac{V_{\text{bus(p-p)}}}{V_{\text{o(rms)}}}$

- The transmission contains:
  - Total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
  - Clock frequency = 50 kHz
  - Repetition burst rate = 400 Hz
  - Maximum bus signal amplitude = 5 V (p-p).
- The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, –6 dB and –15 dB.
- Attack time constant = C<sub>AV</sub> × R<sub>att</sub>.

$$C_{AV} \times 0.76 \text{ V} \left( 10^{\frac{-G_1}{20}} - 10^{\frac{-G_2}{20}} \right)$$

- Decay time =  $\frac{\text{[Equation]}}{I_{\text{dec}}}$

Example: C<sub>AV</sub> = 4.7 μF; I<sub>dec</sub> = 2 μA; G<sub>1</sub> = –9 dB; G<sub>2</sub> = +6 dB → decay time results in 4.14 s.

- When reset is active the GMU-bit (general mute) and the LMU-bit (LINE OUT mute) is set and the I<sup>2</sup>C-bus receiver is in the reset position.
- The AC characteristics are in accordance with the I<sup>2</sup>C-bus specification. The maximum clock frequency is 100 kHz. Information about the I<sup>2</sup>C-bus can be found in the brochure "The I<sup>2</sup>C-bus and how to use it" (order number 9398 393 40011).

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## I<sup>2</sup>C-BUS PROTOCOL

### I<sup>2</sup>C-bus format to read (slave transmits data)

|   |               |     |   |      |    |      |   |
|---|---------------|-----|---|------|----|------|---|
| S | SLAVE ADDRESS | R/W | A | DATA | MA | DATA | P |
|---|---------------|-----|---|------|----|------|---|

**Table 1** Explanation of I<sup>2</sup>C-bus format to read (slave transmits data)

| NAME                         | DESCRIPTION                              |
|------------------------------|--|
| S                            | START condition; generated by the master |
| Standard SLAVE ADDRESS (MAD) | 101 101 1                                |
| R/W                          | 1 (read); generated by the master        |
| A                            | acknowledge; generated by the slave      |
| DATA                         | slave transmits an 8-bit data word       |
| MA                           | acknowledge; generated by the master     |
| P                            | STOP condition; generated by the master  |

**Table 2** Definition of the transmitted bytes after read condition

| FUNCTION         | BYTE | MSB |      |     |     |     |     |     |     | LSB |
|------------------|------|-----|------|-----|-----|-----|-----|-----|-----|-----|
|                  |      | D7  | D6   | D5  | D4  | D3  | D2  | D1  | D0  |     |
| Alignment read 1 | ALR1 | Y   | SAPP | STP | A14 | A13 | A12 | A11 | A10 |     |
| Alignment read 2 | ALR2 | Y   | SAPP | STP | A24 | A23 | A22 | A21 | A20 |     |

**Table 3** Function of the bits in Table 2

| BITS       | FUNCTION  |
|------------|---|
| STP        | stereo pilot identification (stereo received = 1) |
| SAPP       | SAP pilot identification (SAP received = 1)       |
| A1X to A2X | stereo alignment read data                        |
| A1X        | for wideband expander                             |
| A2X        | for spectral expander                             |
| Y          | indefinite  |

The master generates an acknowledge when it has received the first data word ALR1, then the slave transmits the next data word ALR2. Afterwards the master generates an acknowledge, then the slave begins transmitting the first data word ALR1 etc. until the master generates no acknowledge and transmits a STOP condition.

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## I<sup>2</sup>C-bus format to write (slave receives data)

|   |               |     |   |            |   |      |   |   |
|---|---------------|-----|---|------------|---|------|---|---|
| S | SLAVE ADDRESS | R/W | A | SUBADDRESS | A | DATA | A | P |
|---|---------------|-----|---|------------|---|------|---|---|

**Table 4** Explanation of I<sup>2</sup>C-bus format to write (slave receives data)

| NAME                         | DESCRIPTION                         |
|------------------------------|-------------------------------------|
| S                            | START condition                     |
| Standard SLAVE ADDRESS (MAD) | 101 101 1                           |
| R/W                          | 0 (write)                           |
| A                            | acknowledge; generated by the slave |
| SUBADDRESS (SAD)             | see Table 5                         |
| DATA                         | see Table 6                         |
| P                            | STOP condition                      |

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 5 is performed.

**Table 5** Subaddress second byte after MAD

| FUNCTION           | REGISTER | MSB |    |    |    |    |    |    |    | LSB |
|--------------------|----------|-----|----|----|----|----|----|----|----|-----|
|                    |          | D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0 |     |
| Volume right       | VR       | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |     |
| Volume left        | VL       | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1  |     |
| Control 1 (note 1) | CON1     | 0   | 0  | 0  | 0  | 0  | 1  | 0  | 1  |     |
| Control 2          | CON2     | 0   | 0  | 0  | 0  | 0  | 1  | 1  | 0  |     |
| Control 3          | CON3     | 0   | 0  | 0  | 0  | 0  | 1  | 1  | 1  |     |
| Alignment 1        | ALI1     | 0   | 0  | 0  | 0  | 1  | 0  | 0  | 0  |     |
| Alignment 2        | ALI2     | 0   | 0  | 0  | 0  | 1  | 0  | 0  | 1  |     |
| Alignment 3        | ALI3     | 0   | 0  | 0  | 0  | 1  | 0  | 1  | 0  |     |

### Note

1. In auto-increment mode it is necessary to insert 3 dummy data words between volume left and control 1.

**Table 6** Definition of third byte, third byte after MAD and SAD

| FUNCTION     | REGISTER | MSB |        |      |     |     |     |     |     | LSB |
|--------------|----------|-----|--------|------|-----|-----|-----|-----|-----|-----|
|              |          | D7  | D6     | D5   | D4  | D3  | D2  | D1  | D0  |     |
| Volume right | VR       | 0   | VR6    | VR5  | VR4 | VR3 | VR2 | VR1 | VR0 |     |
| Volume left  | VL       | 0   | VL6    | VL5  | VL4 | VL3 | VL2 | VL1 | VL0 |     |
| Control 1    | CON1     | GMU | AVLON  | LOFF | CCD | 0   | SC2 | SC1 | SC0 |     |
| Control 2    | CON2     | SAP | STEREO | TZCM | 1   | LMU | EF2 | EF1 | EF0 |     |
| Control 3    | CON3     | 0   | 0      | 0    | 0   | L3  | L2  | L1  | L0  |     |
| Alignment 1  | ALI1     | 0   | 0      | 0    | A14 | A13 | A12 | A11 | A10 |     |
| Alignment 2  | ALI2     | STS | 0      | 0    | A24 | A23 | A22 | A21 | A20 |     |
| Alignment 3  | ALI3     | ADJ | AT1    | AT2  | 0   | 1   | TC2 | TC1 | TC0 |     |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

**Table 7** Function of the bits in Table 6

| <b>BITS</b> | <b>FUNCTION</b>   |
|-------------|---|
| VR0 to VR6  | volume control right  |
| VL0 to VL6  | volume control left   |
| GMU         | mute control for all outputs (generate mute)                          |
| AVLON       | AVL <b>on/off</b>   |
| CCD         | increased AVL decay current <b>on/off</b>                             |
| LOFF        | switch loudness <b>on/off</b>   |
| SC0 to SC2  | selection between line in and line out                                |
| STEREO, SAP | mode selection for line out   |
| TZCM        | zero cross mode in mute operation (right and left output stage)       |
| LMU         | mute control for line out   |
| EF0 to EF2  | selection between mono, stereo linear, spatial stereo and pseudo mode |
| L0 to L3    | input level adjustment  |
| ADJ         | stereo adjustment <b>on/off</b>                                       |
| A1X to A2X  | stereo alignment data   |
| A1X         | for wideband expander   |
| A2X         | for spectral expander   |
| AT1 and AT2 | attack time at AVL  |
| TC0 to TC2  | timing current alignment data   |
| STS         | stereo level switch   |

**Table 8** Volume setting

| <b>FUNCTION<br/>G<sub>v</sub> (dB)</b> | <b>DATA</b> |           |           |           |           |           |           |
|--|-------------|-----------|-----------|-----------|-----------|-----------|-----------|
|  | <b>V6</b>   | <b>V5</b> | <b>V4</b> | <b>V3</b> | <b>V2</b> | <b>V1</b> | <b>V0</b> |
| 16                                     | 1           | 1         | 1         | 1         | 1         | 1         | 1         |
| 15                                     | 1           | 1         | 1         | 1         | 1         | 1         | 0         |
| 14                                     | 1           | 1         | 1         | 1         | 1         | 0         | 1         |
| 13                                     | 1           | 1         | 1         | 1         | 1         | 0         | 0         |
| 12                                     | 1           | 1         | 1         | 1         | 0         | 1         | 1         |
| 11                                     | 1           | 1         | 1         | 1         | 0         | 1         | 0         |
| 10                                     | 1           | 1         | 1         | 1         | 0         | 0         | 1         |
| 9                                      | 1           | 1         | 1         | 1         | 0         | 0         | 0         |
| 8                                      | 1           | 1         | 1         | 0         | 1         | 1         | 1         |
| 7                                      | 1           | 1         | 1         | 0         | 1         | 1         | 0         |
| 6                                      | 1           | 1         | 1         | 0         | 1         | 0         | 1         |
| 5                                      | 1           | 1         | 1         | 0         | 1         | 0         | 0         |
| 4                                      | 1           | 1         | 1         | 0         | 0         | 1         | 1         |
| 3                                      | 1           | 1         | 1         | 0         | 0         | 1         | 0         |
| 2                                      | 1           | 1         | 1         | 0         | 0         | 0         | 1         |
| 1                                      | 1           | 1         | 1         | 0         | 0         | 0         | 0         |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| FUNCTION<br>G <sub>v</sub> (dB) | DATA |    |    |    |    |    |    |
|---------------------------------|------|----|----|----|----|----|----|
|                                 | V6   | V5 | V4 | V3 | V2 | V1 | V0 |
| 0                               | 1    | 1  | 0  | 1  | 1  | 1  | 1  |
| -1                              | 1    | 1  | 0  | 1  | 1  | 1  | 0  |
| -2                              | 1    | 1  | 0  | 1  | 1  | 0  | 1  |
| -3                              | 1    | 1  | 0  | 1  | 1  | 0  | 0  |
| -4                              | 1    | 1  | 0  | 1  | 0  | 1  | 1  |
| -5                              | 1    | 1  | 0  | 1  | 0  | 1  | 0  |
| -6                              | 1    | 1  | 0  | 1  | 0  | 0  | 1  |
| -7                              | 1    | 1  | 0  | 1  | 0  | 0  | 0  |
| -8                              | 1    | 1  | 0  | 0  | 1  | 1  | 1  |
| -9                              | 1    | 1  | 0  | 0  | 1  | 1  | 0  |
| -10                             | 1    | 1  | 0  | 0  | 1  | 0  | 1  |
| -11                             | 1    | 1  | 0  | 0  | 1  | 0  | 0  |
| -12                             | 1    | 1  | 0  | 0  | 0  | 1  | 1  |
| -13                             | 1    | 1  | 0  | 0  | 0  | 1  | 0  |
| -14                             | 1    | 1  | 0  | 0  | 0  | 0  | 1  |
| -15                             | 1    | 1  | 0  | 0  | 0  | 0  | 0  |
| -16                             | 1    | 0  | 1  | 1  | 1  | 1  | 1  |
| -17                             | 1    | 0  | 1  | 1  | 1  | 1  | 0  |
| -18                             | 1    | 0  | 1  | 1  | 1  | 0  | 1  |
| -19                             | 1    | 0  | 1  | 1  | 1  | 0  | 0  |
| -20                             | 1    | 0  | 1  | 1  | 0  | 1  | 1  |
| -21                             | 1    | 0  | 1  | 1  | 0  | 1  | 0  |
| -22                             | 1    | 0  | 1  | 1  | 0  | 0  | 1  |
| -23                             | 1    | 0  | 1  | 1  | 0  | 0  | 0  |
| -24                             | 1    | 0  | 1  | 0  | 1  | 1  | 1  |
| -25                             | 1    | 0  | 1  | 0  | 1  | 1  | 0  |
| -26                             | 1    | 0  | 1  | 0  | 1  | 0  | 1  |
| -27                             | 1    | 0  | 1  | 0  | 1  | 0  | 0  |
| -28                             | 1    | 0  | 1  | 0  | 0  | 1  | 1  |
| -29                             | 1    | 0  | 1  | 0  | 0  | 1  | 0  |
| -30                             | 1    | 0  | 1  | 0  | 0  | 0  | 1  |
| -31                             | 1    | 0  | 1  | 0  | 0  | 0  | 0  |
| -32                             | 1    | 0  | 0  | 1  | 1  | 1  | 1  |
| -33                             | 1    | 0  | 0  | 1  | 1  | 1  | 0  |
| -34                             | 1    | 0  | 0  | 1  | 1  | 0  | 1  |
| -35                             | 1    | 0  | 0  | 1  | 1  | 0  | 0  |
| -36                             | 1    | 0  | 0  | 1  | 0  | 1  | 1  |
| -37                             | 1    | 0  | 0  | 1  | 0  | 1  | 0  |
| -38                             | 1    | 0  | 0  | 1  | 0  | 0  | 1  |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

| FUNCTION<br>G <sub>v</sub> (dB) | DATA |    |    |    |    |    |    |
|---------------------------------|------|----|----|----|----|----|----|
|                                 | V6   | V5 | V4 | V3 | V2 | V1 | V0 |
| -39                             | 1    | 0  | 0  | 1  | 0  | 0  | 0  |
| -40                             | 1    | 0  | 0  | 0  | 1  | 1  | 1  |
| -41                             | 1    | 0  | 0  | 0  | 1  | 1  | 0  |
| -42                             | 1    | 0  | 0  | 0  | 1  | 0  | 1  |
| -43                             | 1    | 0  | 0  | 0  | 1  | 0  | 0  |
| -44                             | 1    | 0  | 0  | 0  | 0  | 1  | 1  |
| -45                             | 1    | 0  | 0  | 0  | 0  | 1  | 0  |
| -46                             | 1    | 0  | 0  | 0  | 0  | 0  | 1  |
| -47                             | 1    | 0  | 0  | 0  | 0  | 0  | 0  |
| -48                             | 0    | 1  | 1  | 1  | 1  | 1  | 1  |
| -49                             | 0    | 1  | 1  | 1  | 1  | 1  | 0  |
| -50                             | 0    | 1  | 1  | 1  | 1  | 0  | 1  |
| -51                             | 0    | 1  | 1  | 1  | 1  | 0  | 0  |
| -52                             | 0    | 1  | 1  | 1  | 0  | 1  | 1  |
| -53                             | 0    | 1  | 1  | 1  | 0  | 1  | 0  |
| -54                             | 0    | 1  | 1  | 1  | 0  | 0  | 1  |
| -55                             | 0    | 1  | 1  | 1  | 0  | 0  | 0  |
| -56                             | 0    | 1  | 1  | 0  | 1  | 1  | 1  |
| -57                             | 0    | 1  | 1  | 0  | 1  | 1  | 0  |
| -58                             | 0    | 1  | 1  | 0  | 1  | 0  | 1  |
| -59                             | 0    | 1  | 1  | 0  | 1  | 0  | 0  |
| -60                             | 0    | 1  | 1  | 0  | 0  | 1  | 1  |
| -61                             | 0    | 1  | 1  | 0  | 0  | 1  | 0  |
| -62                             | 0    | 1  | 1  | 0  | 0  | 0  | 1  |
| -63                             | 0    | 1  | 1  | 0  | 0  | 0  | 0  |
| -64                             | 0    | 1  | 0  | 1  | 1  | 1  | 1  |
| -65                             | 0    | 1  | 0  | 1  | 1  | 1  | 0  |
| -66                             | 0    | 1  | 0  | 1  | 1  | 0  | 1  |
| -67                             | 0    | 1  | 0  | 1  | 1  | 0  | 0  |
| -68                             | 0    | 1  | 0  | 1  | 0  | 1  | 1  |
| -69                             | 0    | 1  | 0  | 1  | 0  | 1  | 0  |
| -70                             | 0    | 1  | 0  | 1  | 0  | 0  | 1  |
| -71                             | 0    | 1  | 0  | 1  | 0  | 0  | 0  |
| Mute                            | 0    | 1  | 0  | 0  | 1  | 1  | 1  |



# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

**Table 9** Loudness setting

| CHARACTERISTIC | DATA LOFF |
|----------------|-----------|
| With loudness  | 0         |
| Linear         | 1         |

**Table 10** Effects setting

| FUNCTION                                    | DATA |     |     |
|---|------|-----|-----|
|   | EF2  | EF1 | EF0 |
| Stereo linear <b>on</b>                     | 0    | 0   | 0   |
| Pseudo <b>on</b>                            | 0    | 0   | 1   |
| Spatial stereo;<br>30% anti-phase crosstalk | 0    | 1   | 0   |
| Spatial stereo;<br>50% anti-phase crosstalk | 0    | 1   | 1   |
| Forced mono                                 | 1    | 1   | 1   |

**Table 11** Selector setting

| FUNCTION <sup>(1)</sup> | DATA |     |     |
|-------------------------|------|-----|-----|
|                         | SC2  | SC1 | SC0 |
| Inputs LOR and LOL      | 0    | 0   | 0   |
| Inputs LOR and LOR      | 0    | 0   | 1   |
| Inputs LOL and LOL      | 0    | 1   | 0   |
| Inputs LOL and LOR      | 0    | 1   | 1   |
| Inputs LIR and LIL      | 1    | 0   | 0   |
| Inputs LIR and LIR      | 1    | 0   | 1   |
| Inputs LIL and LIL      | 1    | 1   | 0   |
| Inputs LIL and LIR      | 1    | 1   | 1   |

**Note**

1. Input connected to outputs SOR and SOL.

**Table 12** Switch setting at line out

| LINE OUT SIGNALS AT |       | DATA<br>TRANSMISSION STATUS<br>INTERNAL SWITCH, READABLE BITS: STP, SAPP | SETTING BITS |     |
|---------------------|-------|--|--------------|-----|
| LOL                 | LOR   |  | STEREO       | SAP |
| SAP                 | SAP   | SAP received   | 1            | 1   |
| Mute                | mute  | no SAP received  | 1            | 1   |
| Left                | right | STEREO received  | 1            | 0   |
| Mono                | mono  | no STEREO received   | 1            | 0   |
| Mono                | SAP   | SAP received   | 0            | 1   |
| Mono                | mute  | no SAP received  | 0            | 1   |
| Mono                | mono  | independent  | 0            | 0   |

**Table 13** Zero cross detection setting

| FUNCTION  | DATA TZCM |
|---|-----------|
| Direct mute control                               | 0         |
| Mute control delayed until the next zero crossing | 1         |

**Table 14** Mute setting

| FUNCTION                           | DATA GMU | FUNCTION                            | DATA LMU |
|------------------------------------|----------|-------------------------------------|----------|
| Forced mute at OUTR, OUTL and OUTS | 1        | forced mute at LOR and LOL          | 1        |
| Audio processor controlled outputs | 0        | stereo processor controlled outputs | 0        |

I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

**Table 15** AVL attack time

| FUNCTION                  | DATA |     |
|---------------------------|------|-----|
|                           | AT1  | AT2 |
| R <sub>att</sub> = 420 Ω  | 0    | 0   |
| R <sub>att</sub> = 730 Ω  | 1    | 0   |
| R <sub>att</sub> = 1200 Ω | 0    | 1   |
| R <sub>att</sub> = 2100 Ω | 1    | 1   |

**Table 16** ADJ bit setting

| FUNCTION                              | DATA |
|---------------------------------------|------|
| Stereo decoder operation mode         | 0    |
| Auto adjustment of channel separation | 1    |

**Table 17** AVLON bit setting

| FUNCTION                            | DATA |
|-------------------------------------|------|
| Automatic volume control <b>off</b> | 0    |
| Automatic volume control <b>on</b>  | 1    |

**Table 18** CCD bit setting

| FUNCTION                               | DATA |
|--|------|
| Load current for normal AVL decay time | 0    |
| Increased load current                 | 1    |

**Table 19** STS bit setting (pilot threshold stereo on)

| FUNCTION                 | DATA |
|--------------------------|------|
| ST <sub>on</sub> ≤ 35 mV | 1    |
| ST <sub>on</sub> ≤ 30 mV | 0    |

**Table 20** Timing current setting

| FUNCTION<br>I <sub>s</sub> RANGE | DATA |     |     |
|----------------------------------|------|-----|-----|
|                                  | TC2  | TC1 | TC0 |
| +30%                             | 1    | 0   | 0   |
| +20%                             | 1    | 0   | 1   |
| +10%                             | 1    | 1   | 0   |
| Nominal                          | 0    | 1   | 1   |
| -10%                             | 0    | 1   | 0   |
| -20%                             | 0    | 0   | 1   |
| -30%                             | 0    | 0   | 0   |

**Table 21** Level adjust setting

| G <sub>L</sub><br>(dB) | DATA |    |    |    |
|------------------------|------|----|----|----|
|                        | L3   | L2 | L1 | L0 |
| +4.0                   | 1    | 1  | 1  | 1  |
| +3.5                   | 1    | 1  | 1  | 0  |
| +3.0                   | 1    | 1  | 0  | 1  |
| +2.5                   | 1    | 1  | 0  | 0  |
| +2.0                   | 1    | 0  | 1  | 1  |
| +1.5                   | 1    | 0  | 1  | 0  |
| +1.0                   | 1    | 0  | 0  | 1  |
| +0.5                   | 1    | 0  | 0  | 0  |
| 0.0                    | 0    | 1  | 1  | 1  |
| -0.5                   | 0    | 1  | 1  | 0  |
| -1.0                   | 0    | 1  | 0  | 1  |
| -1.5                   | 0    | 1  | 0  | 0  |
| -2.0                   | 0    | 0  | 1  | 1  |
| -2.5                   | 0    | 0  | 1  | 0  |
| -3.0                   | 0    | 0  | 0  | 1  |
| -3.5                   | 0    | 0  | 0  | 0  |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

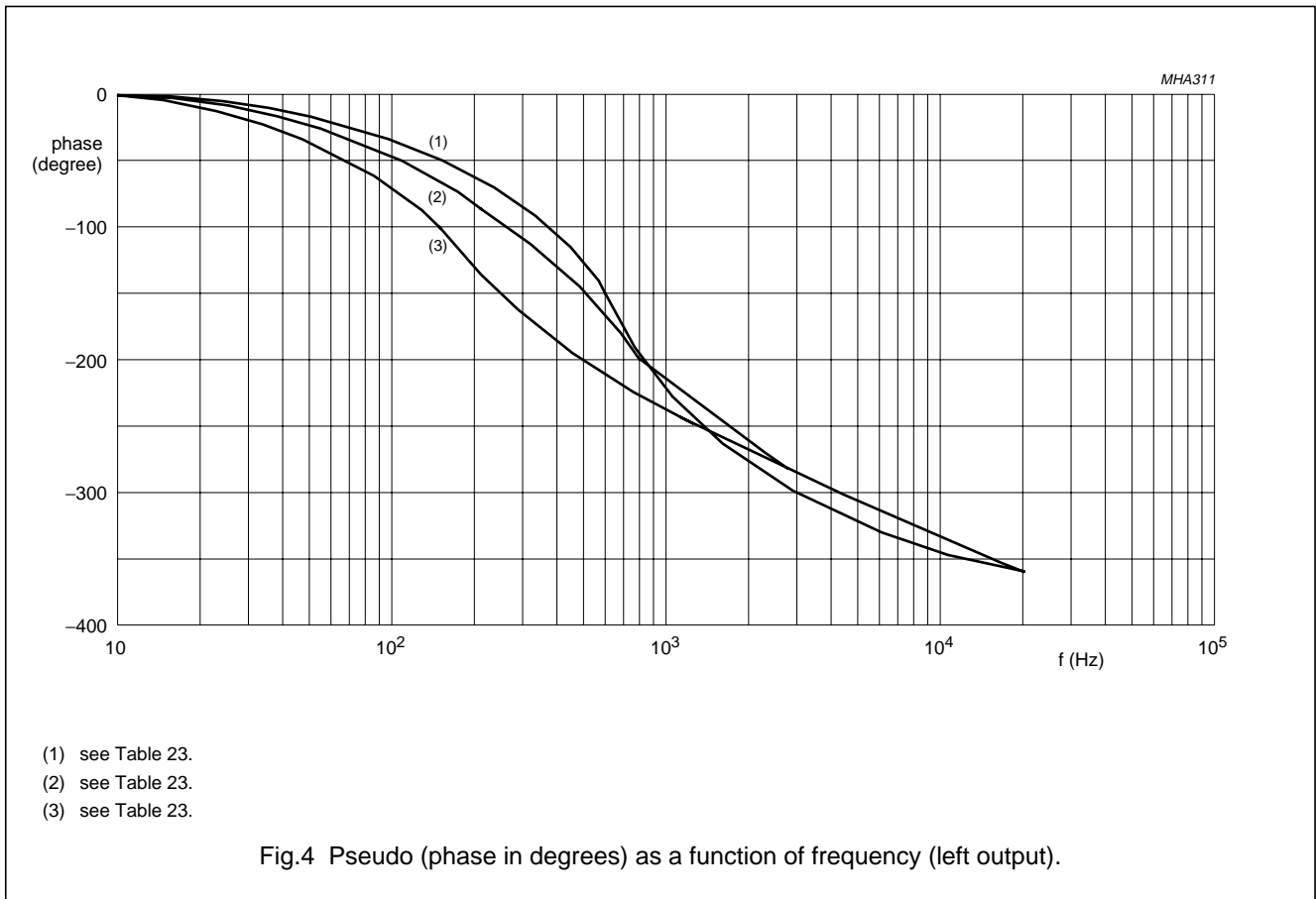
TDA9852

**Table 22** Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2

| FUNCTION      | DATA         |           |           |           |           |
|---------------|--------------|-----------|-----------|-----------|-----------|
|               | D4<br>AX4    | D3<br>AX3 | D2<br>AX2 | D1<br>AX1 | D0<br>AX0 |
| Gain increase | 1            | 1         | 1         | 1         | 1         |
|               | 1            | 1         | 1         | 1         | 0         |
|               | 1            | 1         | 1         | 0         | 1         |
|               | 1            | 1         | 1         | 0         | 0         |
|               | 1            | 1         | 0         | 1         | 1         |
|               | 1            | 1         | 0         | 1         | 0         |
|               | 1            | 1         | 0         | 0         | 1         |
|               | 1            | 1         | 0         | 0         | 0         |
|               | 1            | 0         | 1         | 1         | 1         |
|               | 1            | 0         | 1         | 1         | 0         |
|               | 1            | 0         | 1         | 0         | 0         |
|               | 1            | 0         | 0         | 1         | 1         |
|               | 1            | 0         | 0         | 1         | 0         |
|               | 1            | 0         | 0         | 0         | 1         |
|               | Nominal gain | 1         | 0         | 0         | 0         |
| 0             |              | 1         | 1         | 1         | 1         |
| Gain decrease | 0            | 1         | 1         | 1         | 0         |
|               | 0            | 1         | 1         | 0         | 1         |
|               | 0            | 1         | 1         | 0         | 0         |
|               | 0            | 1         | 0         | 1         | 1         |
|               | 0            | 1         | 0         | 1         | 0         |
|               | 0            | 1         | 0         | 0         | 1         |
|               | 0            | 1         | 0         | 0         | 0         |
|               | 0            | 0         | 1         | 1         | 1         |
|               | 0            | 0         | 1         | 1         | 0         |
|               | 0            | 0         | 1         | 0         | 1         |
|               | 0            | 0         | 1         | 0         | 0         |
|               | 0            | 0         | 0         | 1         | 1         |
|               | 0            | 0         | 0         | 1         | 0         |
|               | 0            | 0         | 0         | 0         | 1         |
|               | 0            | 0         | 0         | 0         | 0         |

I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

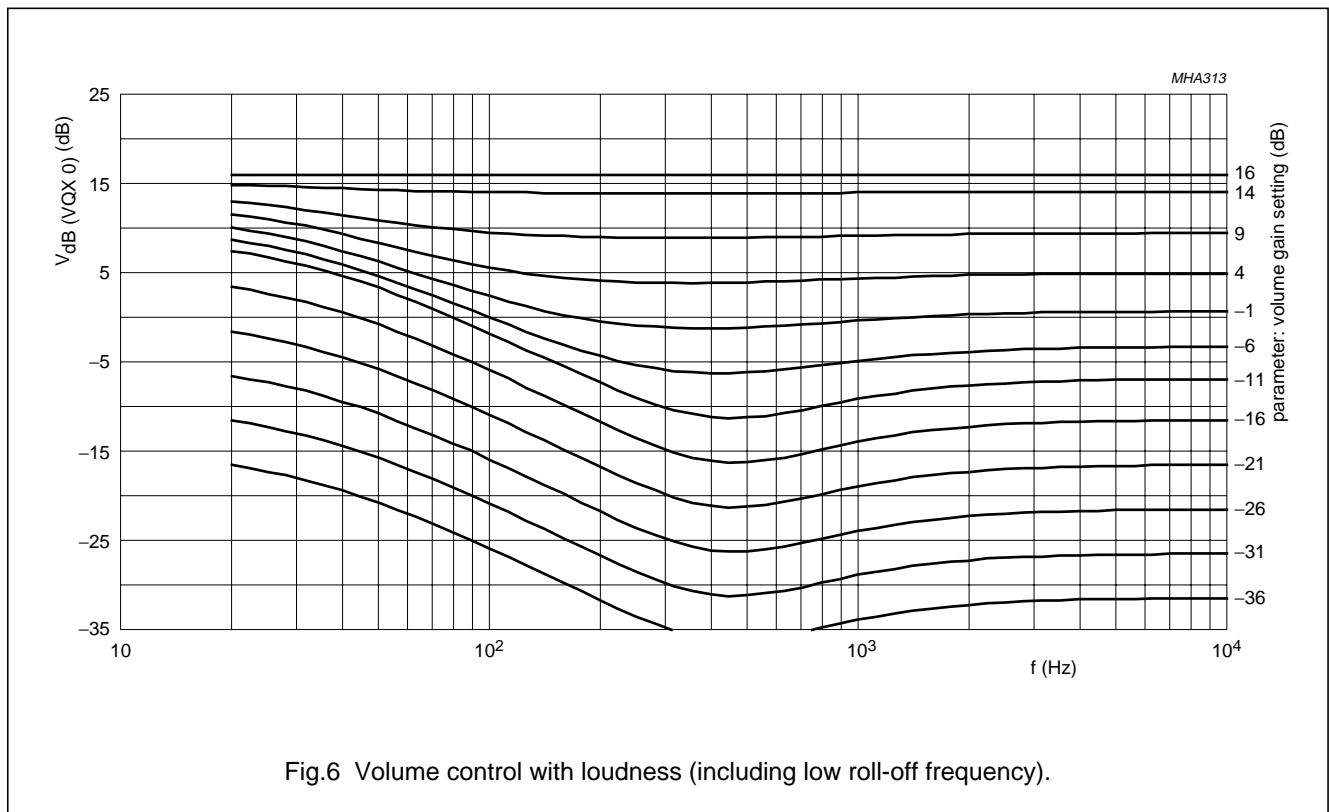
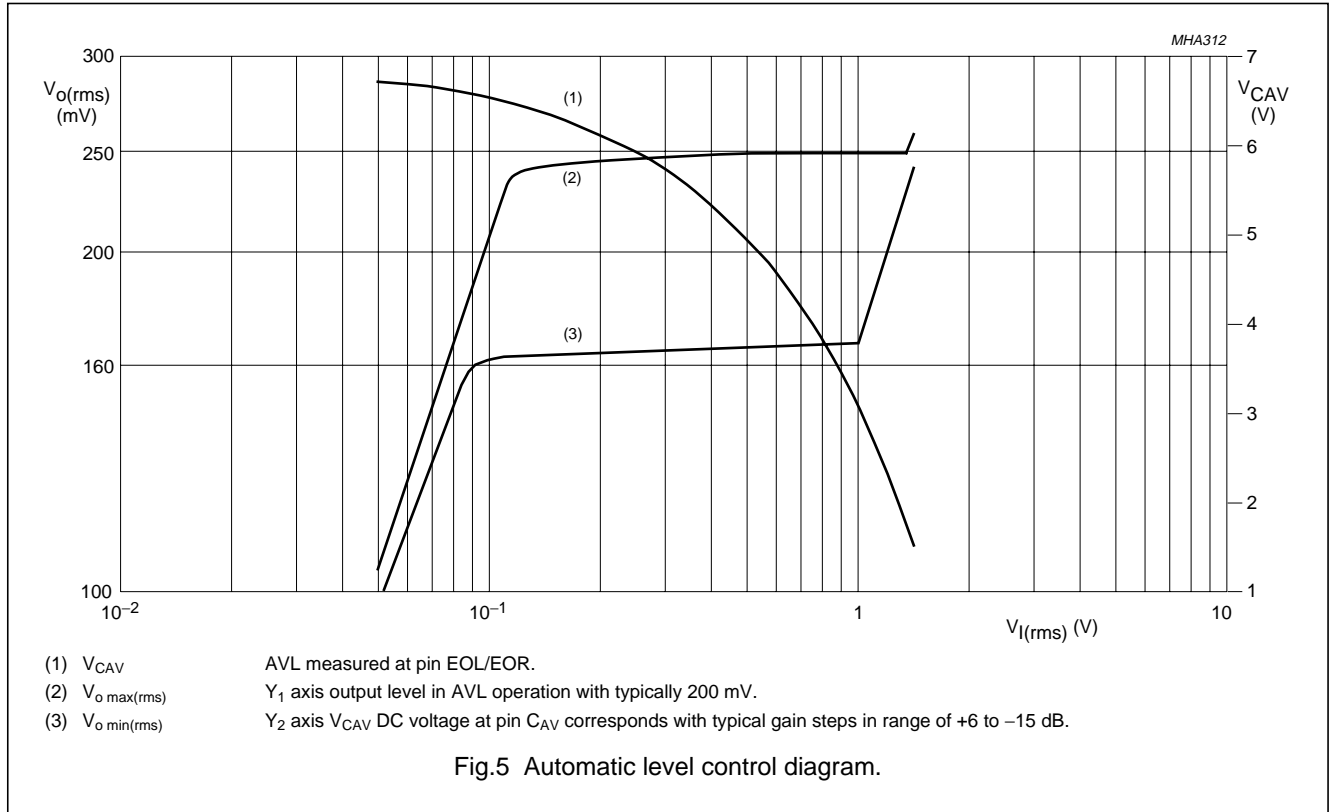


**Table 23** Explanation of curves in Fig.4

| CURVE | CAPACITANCE AT PIN C <sub>PS1</sub><br>(nF) | CAPACITANCE AT PIN C <sub>PS2</sub><br>(nF) | EFFECT           |
|-------|---|---|------------------|
| 1     | 15  | 15  | normal           |
| 2     | 5.6   | 47  | intensified      |
| 3     | 5.6   | 68  | more intensified |

I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

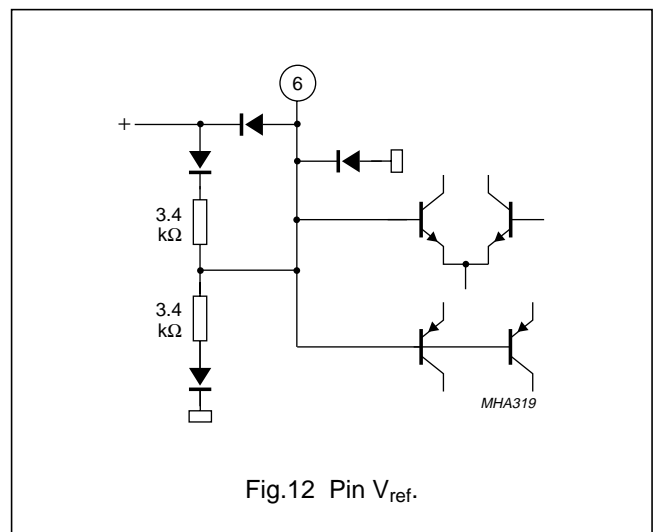
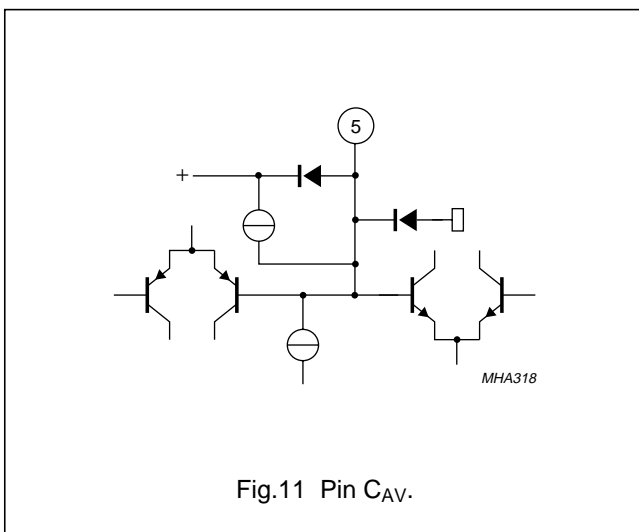
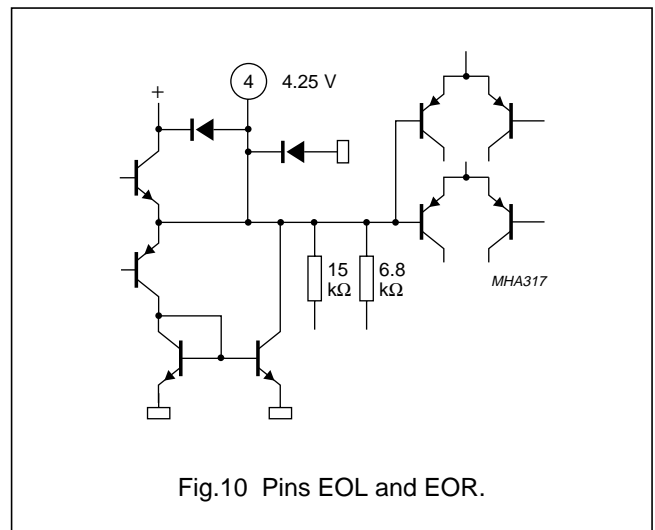
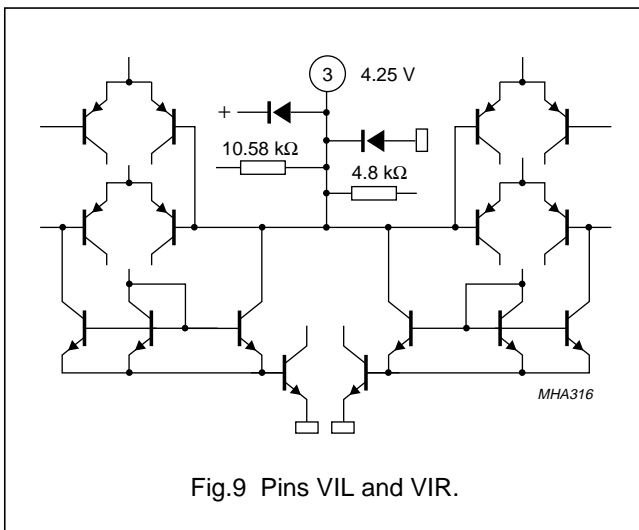
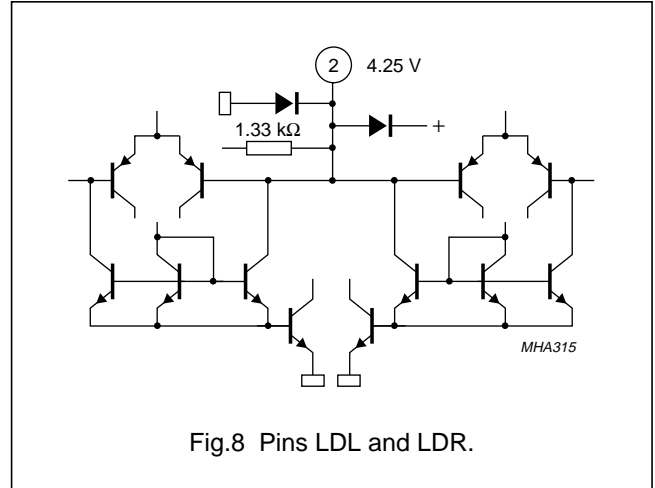
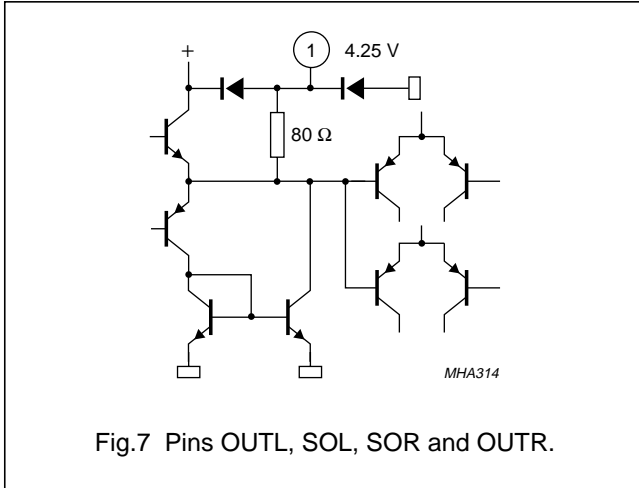
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# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

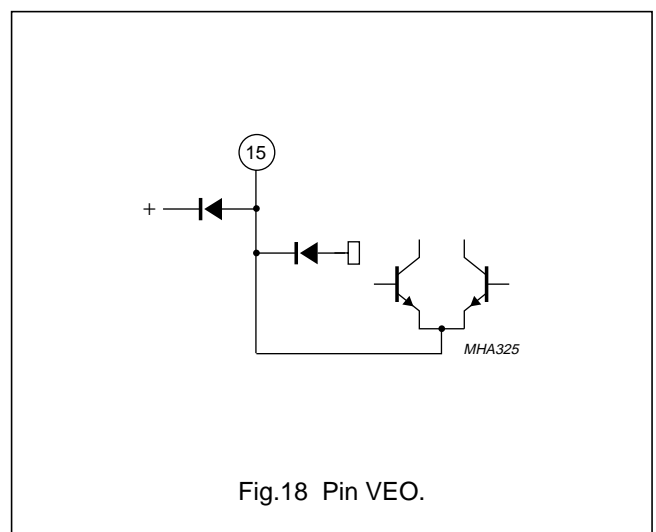
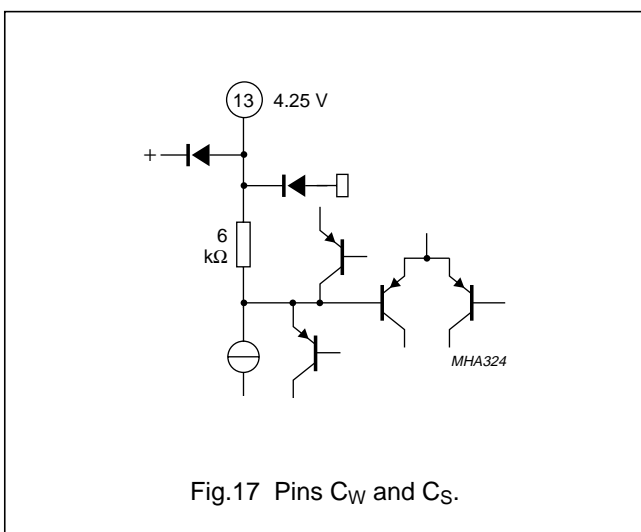
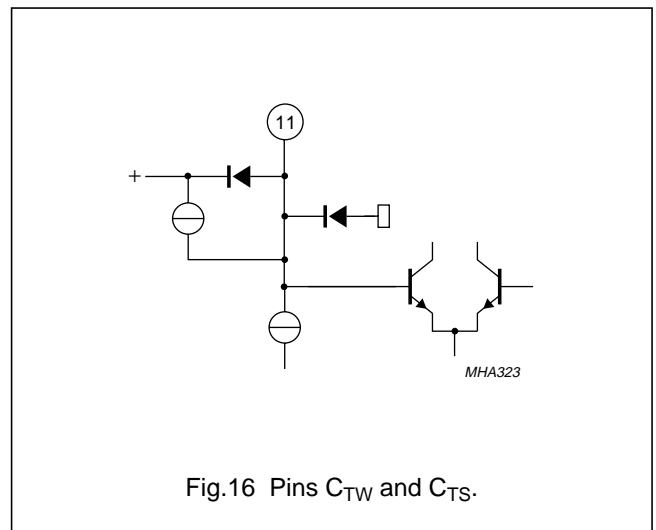
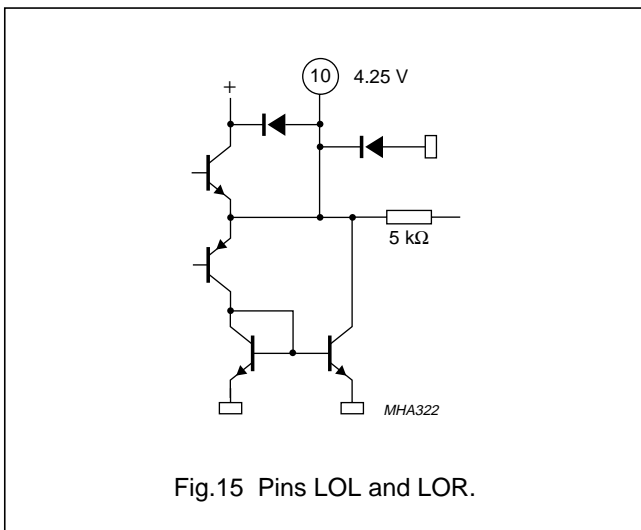
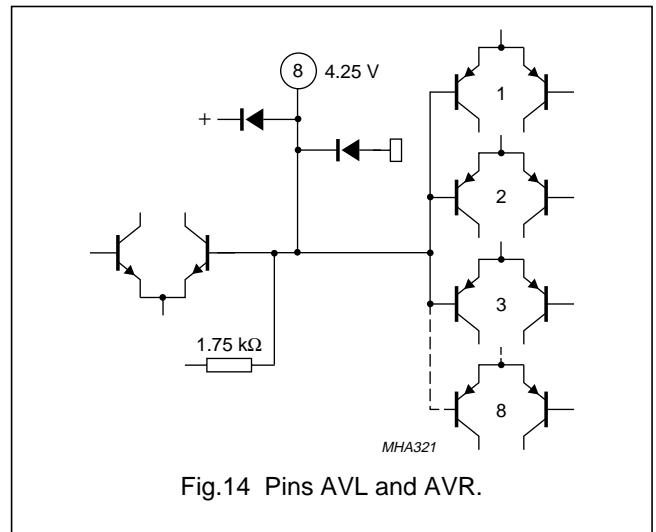
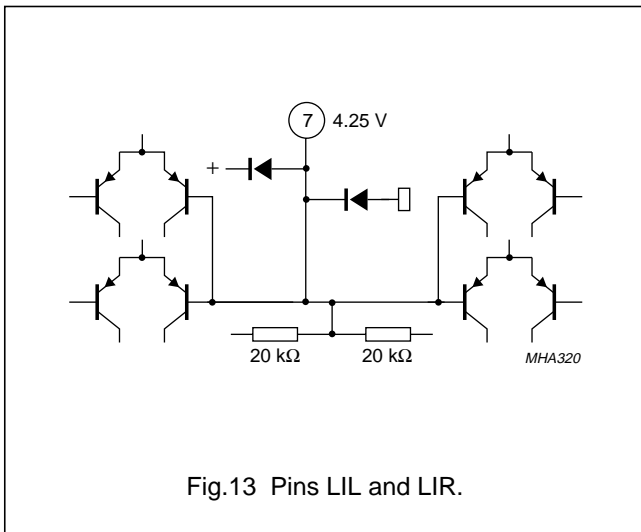
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## INTERNAL PIN CONFIGURATIONS



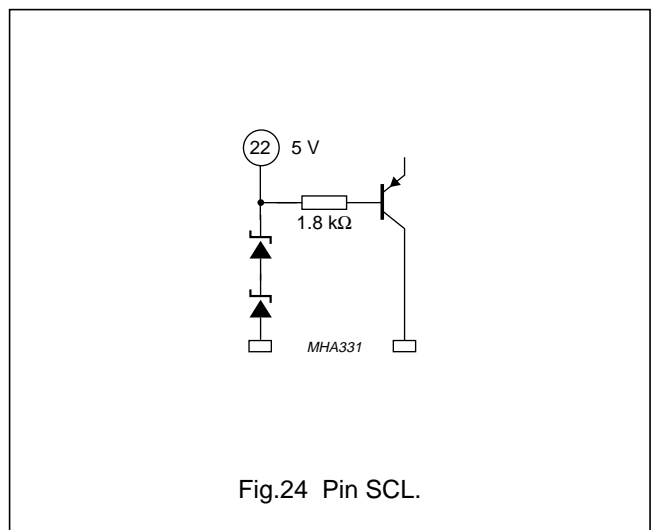
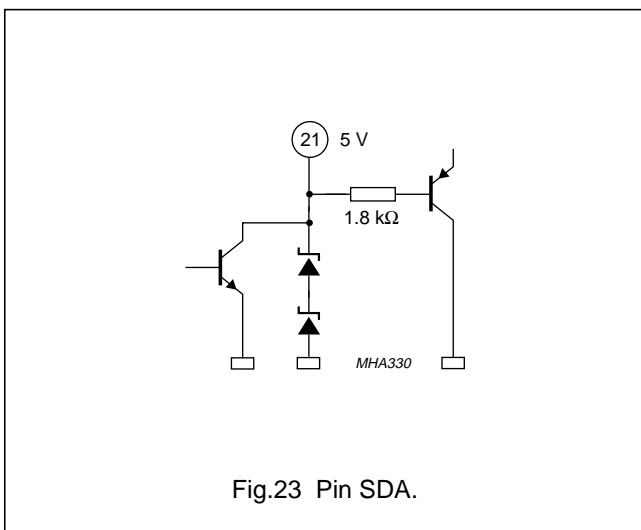
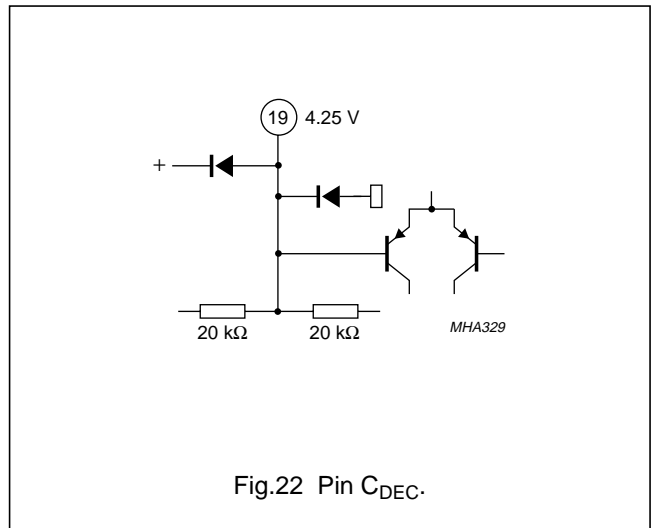
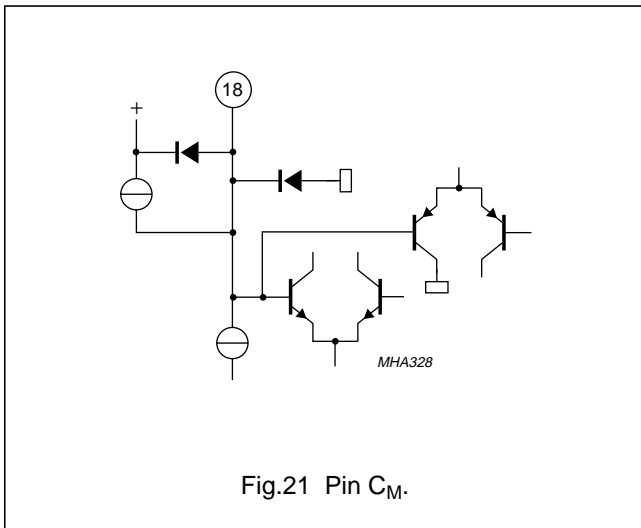
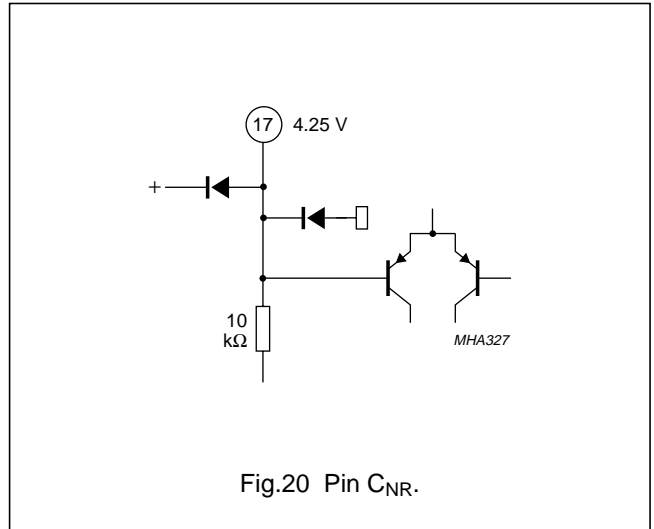
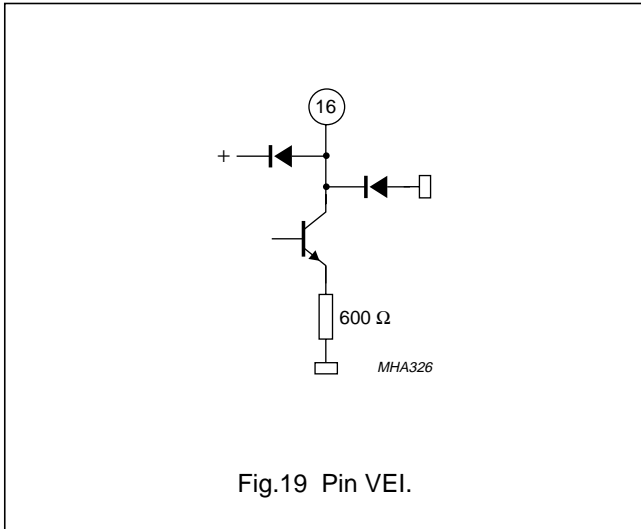
I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

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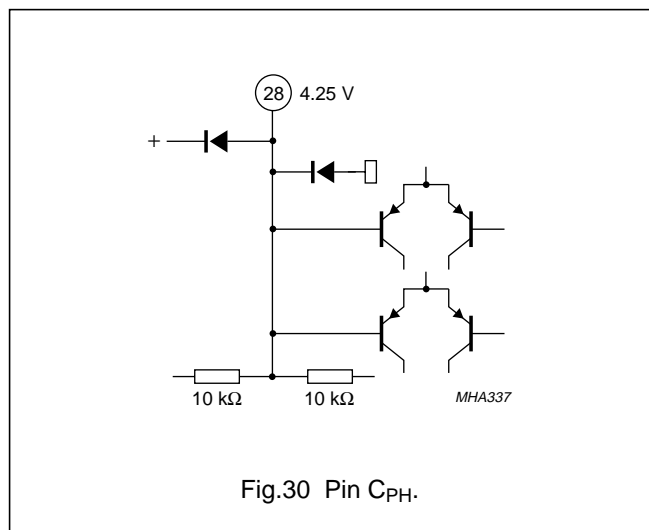
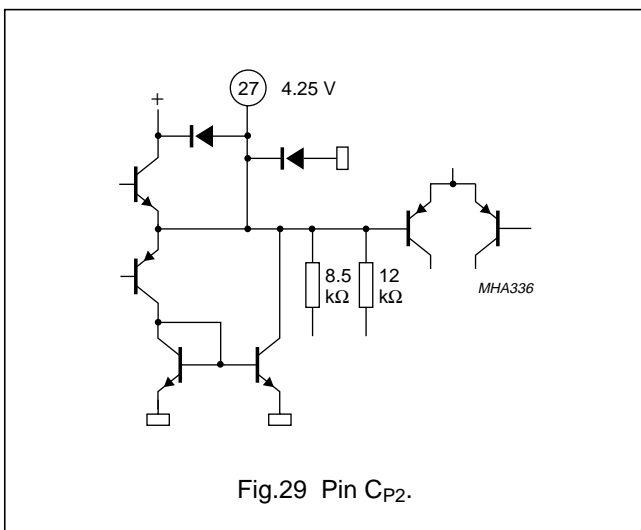
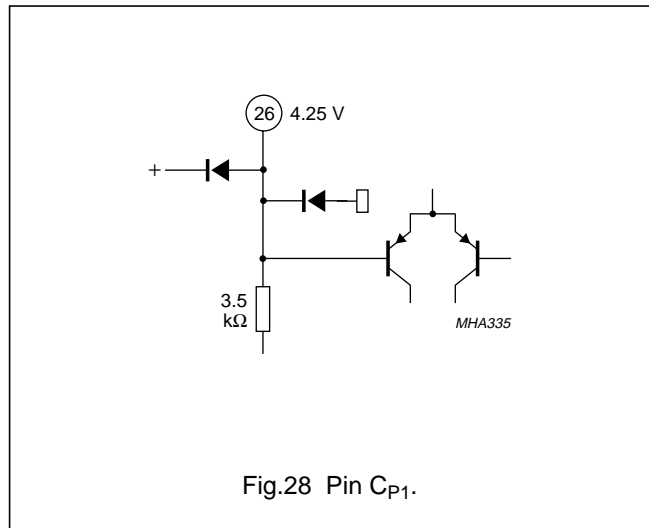
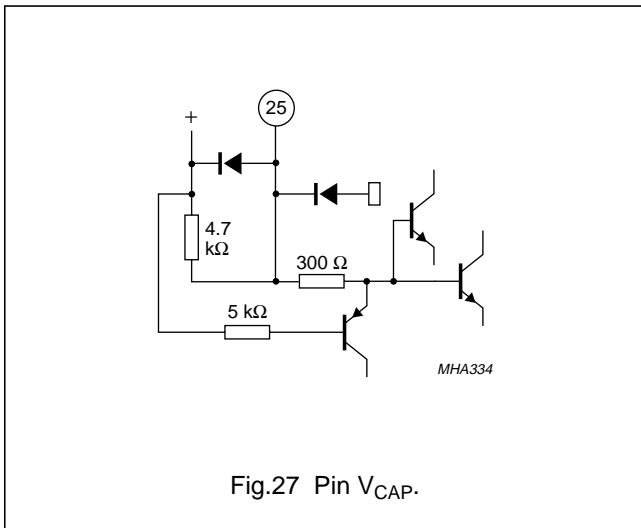
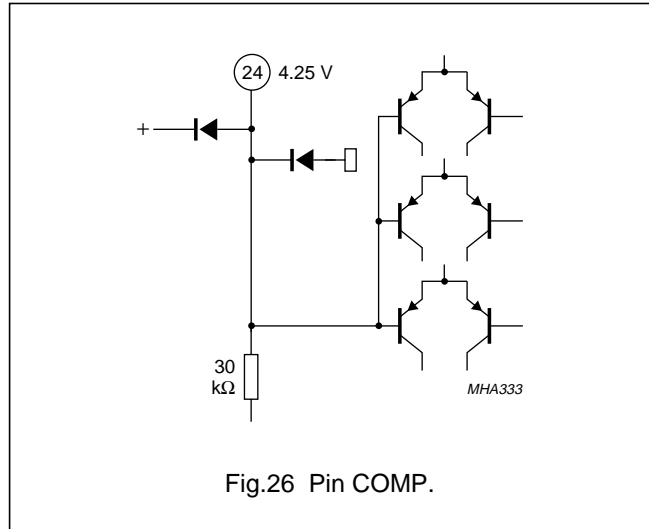
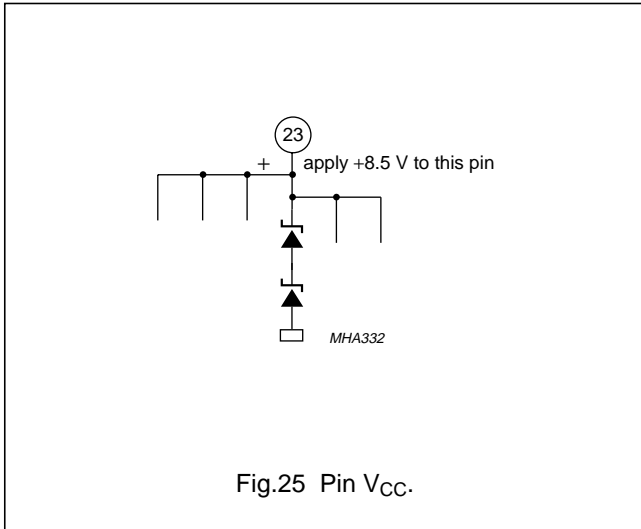
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## TDA9852

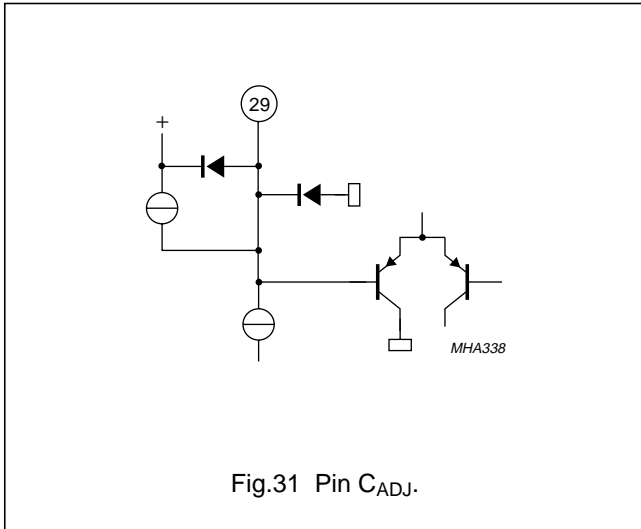


Fig.31 Pin C<sub>ADJ</sub>.

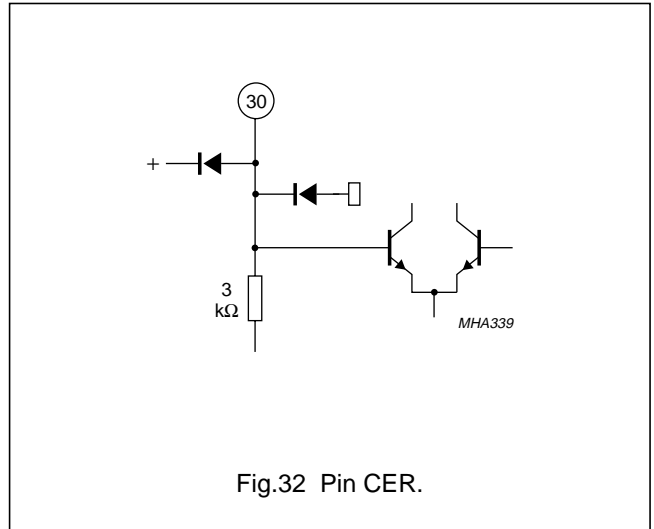


Fig.32 Pin CER.

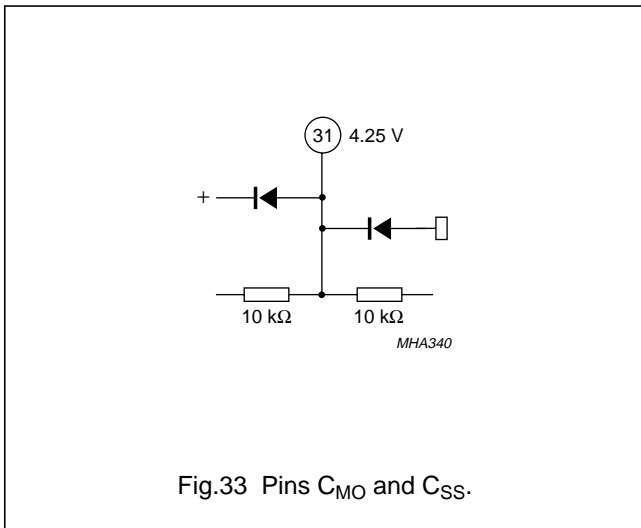


Fig.33 Pins C<sub>MO</sub> and C<sub>SS</sub>.

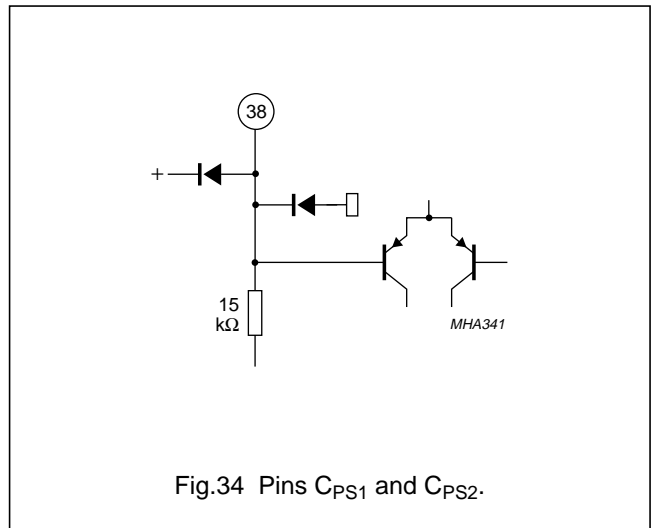


Fig.34 Pins C<sub>PS1</sub> and C<sub>PS2</sub>.

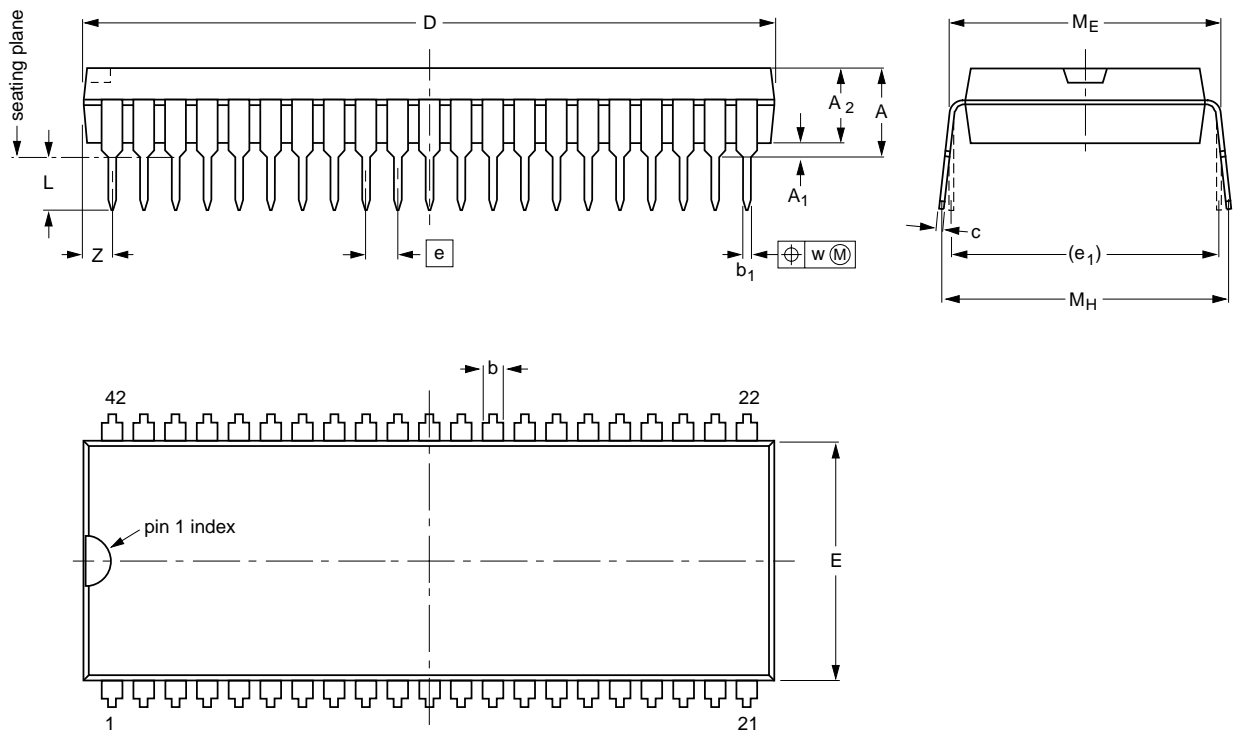
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TDA9852

PACKAGE OUTLINES

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil)

SOT270-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b          | b <sub>1</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | e <sub>1</sub> | L          | M <sub>E</sub> | M <sub>H</sub> | w    | z <sup>(1)</sup> max. |
|------|--------|---------------------|---------------------|------------|----------------|--------------|------------------|------------------|-------|----------------|------------|----------------|----------------|------|-----------------------|
| mm   | 5.08   | 0.51                | 4.0                 | 1.3<br>0.8 | 0.53<br>0.40   | 0.32<br>0.23 | 38.9<br>38.4     | 14.0<br>13.7     | 1.778 | 15.24          | 3.2<br>2.9 | 15.80<br>15.24 | 17.15<br>15.90 | 0.18 | 1.73                  |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

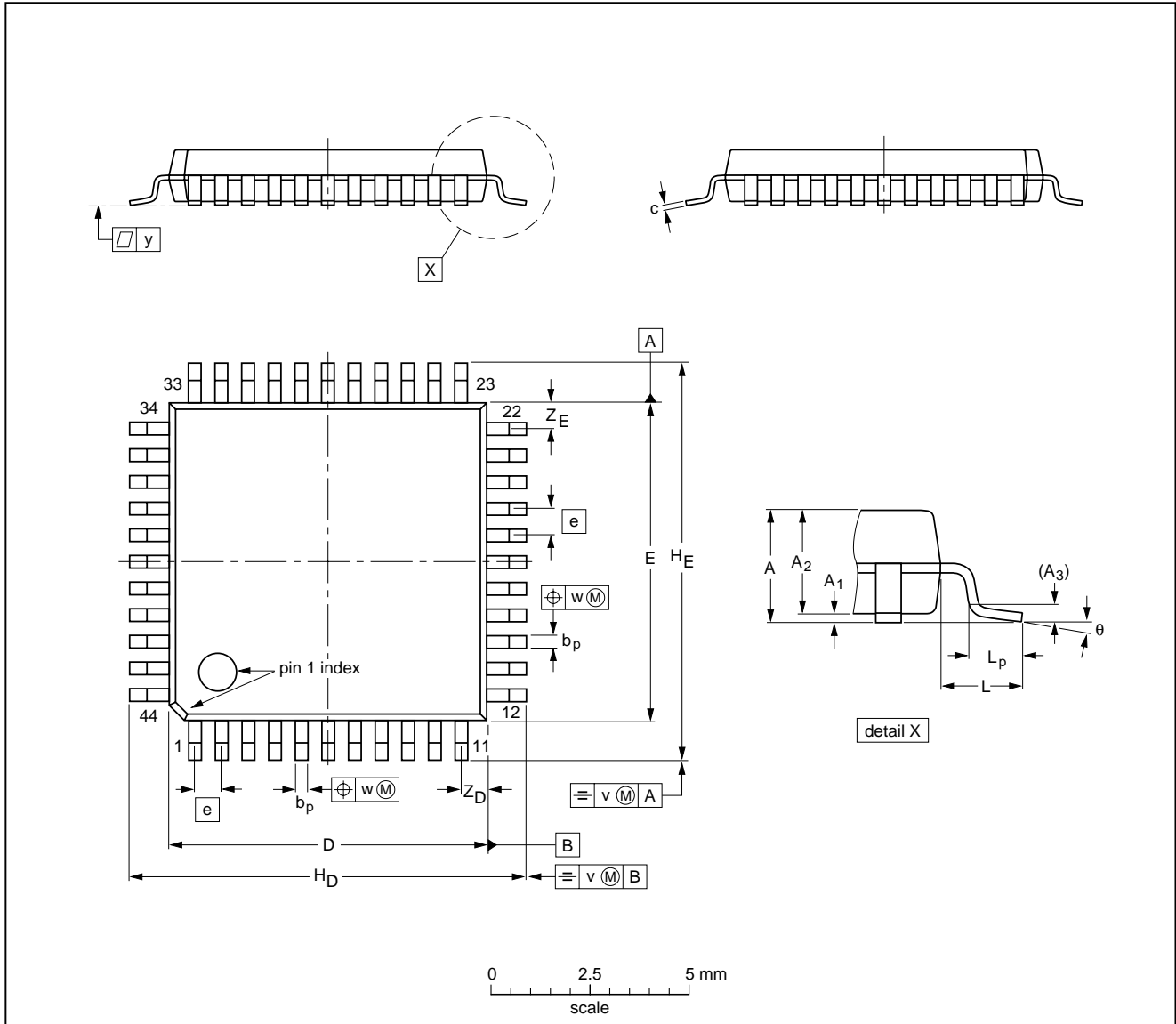
| OUTLINE VERSION | REFERENCES |       |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|-------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC | EIAJ |  |                     |                      |
| SOT270-1        |            |       |      |  |                     | 90-02-13<br>95-02-04 |

I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e   | H <sub>D</sub> | H <sub>E</sub> | L   | L <sub>p</sub> | v    | w    | y   | Z <sub>D</sub> <sup>(1)</sup> | Z <sub>E</sub> <sup>(1)</sup> | θ         |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|------|------|-----|-------------------------------|-------------------------------|-----------|
| mm   | 2.10   | 0.25<br>0.05   | 1.85<br>1.65   | 0.25           | 0.40<br>0.20   | 0.25<br>0.14 | 10.1<br>9.9      | 10.1<br>9.9      | 0.8 | 12.9<br>12.3   | 12.9<br>12.3   | 1.3 | 0.95<br>0.55   | 0.15 | 0.15 | 0.1 | 1.2<br>0.8                    | 1.2<br>0.8                    | 10°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |       |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|-------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC | EIAJ |  |                     |                      |
| SOT307-2        |            |       |      |  |                     | 95-02-04<br>97-08-01 |

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

### SDIP

#### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### QFP

#### REFLOW SOLDERING

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our "Quality Reference Handbook" (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

#### WAVE SOLDERING

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

#### If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

**Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

## DEFINITIONS

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
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**Belgium:** see The Netherlands

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Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
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**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 1949

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580/xxx

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
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**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,  
Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
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Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

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Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

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Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
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